

# Electronic Transport in Graphene: $p$ - $n$ Junctions, Shot Noise, and Nanoribbons

A dissertation presented  
by

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to

The School of Engineering and Applied Sciences  
in partial fulfillment of the requirements  
for the degree of  
Doctor of Philosophy  
in the subject of

Applied Physics

Harvard University  
Cambridge, Massachusetts

May 2009

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## Abstract

Novel, two-dimensional materials have allowed for the inception and elucidation of a plethora of physical phenomena. On such material, a hexagonal lattice of carbon atoms called graphene, is a unique, truly two-dimensional molecular conductor. This thesis describes six experiments that elucidate some interesting physical properties and technological applications of graphene, with an emphasis on graphene-based  $p$ - $n$  junctions.

A technique for the creation of high-quality  $p$ - $n$  junctions of graphene is described. Transport measurements at zero magnetic field demonstrate local control of the carrier type and density bipolar graphene-based junctions. In the quantum Hall regime, new plateaus in the conductance are observed and explained in terms of mode mixing at the  $p$ - $n$  interface.

Shot noise in unipolar and bipolar graphene devices is measured. A density-independent Fano factor is observed, contrary to theoretical expectations. Further, an independence on device geometry is also observed. The role of disorder on the measured Fano factor is discussed, and comparison to recent theory for disordered graphene is made.

The effect of a two-terminal geometry, where the device aspect ratio is different from unity, is measured experimentally and analyzed theoretically. A method for extracting layer number from the conductance extrema is proposed. A method for a conformal mapping of a device with asymmetric contacts to a rectangle is demonstrated. Finally, possible origins of discrepancies between theory and experiment are discussed.

Transport along  $p$ - $n$  junctions in graphene is reported. Enhanced transport along the junction is observed and attributed to states that exist at the  $p$ - $n$  interface. A correspondence between the observed phenomena at low-field and in the quantum Hall regime is

observed. An electric field perpendicular to the junction is found to reduce the enhanced conductance at the  $p$ - $n$  junction. A corollary between the  $p$ - $n$  interface states and “snake states” in an inhomogeneous magnetic field is proposed and its relationship to the minimum conductivity in graphene is discussed.

A final pair of experiments demonstrate how a helium ion microscope can be used to reduce the dimensionality of graphene one further, producing graphene nanoribbons. The effect of etching on transport and doping level of the graphene nanoribbons is discussed.

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# Acknowledgements

Graduate school would have been unbearably long if it weren't for my family, friends and colleagues.

First I would like to thank my advisor, Charlie Marcus. There is nothing as energizing as watching him doing physics. He has an uncanny clairvoyance for research and for what the most interesting experiments are. He has taken me from physics childhood to adulthood, and I will always be grateful for the lessons, advice and humor he shared with me along the way.

Next is Prof. Cynthia Friend. I had the pleasure of working in her research group for a year and picked up some very important tools along the way. Most important was a solid understanding of surface science, much of which played a very important role in the development of the functionalization layer for graphene.

Thanks to Prof. Levitov and Dima Abanin. Their insight into our experiments were essential and we would have been scooped on at least one occasion if it weren't for them. It was a pleasure to work with you both.

Then there are my partners in crime. My first year in graduate school was quite an adjustment but I got a lot of laughs from my workmates. Michael Biercuk and Alex Johnson were nice enough to pummel me with pennies, call me "Jimmah" and make sure everyone in the lab knew about "Peeps". Upon returning to the Marcuslab, I got to know Jeff Miller better, finding out we share a great passion for tea (although he was a black tea guy). Thanks for turning me on the Upton Tea and teaching me that the first pot of good tea should be thrown out. Also, I had a lot of fun running with Edward Laird. Thanks for introducing me to the sport.

Soon after I was introduced to one of the funnest people I've ever met, David Reilly. His impressions and love for all things brown will live in my memory always. He also helped

me get through a lot of tough times, always having something funny to say in the end. Thank you for the Big Mac and The Button, and for showing how good coffee could be. More recently, I had the pleasure of getting to know a few others around lab. Ferdinand Keummeth - Ferdy - you have to be one of the most interesting and intelligent people I've even met. Chrisitian Barthel - Bartel - the most innocently inappropriate and funny person known to physics, thanks for the laughs. Maja Cassidy - Mah Jah - you're the toughest in the lab, hands down. And thanks to Danielle Reuter for sharing her love of photographs with me.

Most importantly, to Leo. If Charlie was my physics-father, you're my physics-older brother. You taught me how to do physics correctly on a day to day basis. You taught me how to be thorough and to be passionate... "I mean come on!" Thanks for everything Leo.

That's just a small slice of the people I've met through the Marcus and Friend Labs. I've learned things from all the lab members I worked with. Thanks to Jason Petta, Dominik Zumbhul, Sang Chu, Abram Falk, Nathaniel Craig, Susan Watson, Andrew Bestwick, Jen Harlow, Hugh Churchill, Yiming Zhang, Doug McClure, Yongie Hu, James Medford, Angela Kou, Patrick Herring, Sandro Erni, Shu Nakaharai, Max Lemme, Tom Baker, Andreas Klust, Xiaoling Liu, Ryan Quiller and Dilini Pinnaduwaage.

Now to friends and family. Kasey Russell, thanks for teaching me about climbing, for always wanting to talk about physics and for being my guitar buddy. Oh ya, and thanks for lending me Trip. Thanks to all the people at Greyhound Welfare, my sanctuary away from physics. Prof. Betty Young, thank you for introducing me to physics and for helping me at the early stages of my physics career.

To Chulo, Mo and Pelo, your silliness kept me smiling when I was sad during graduate school. Thanks to my mom for being a source of strength and inspiration. She taught me about hard work and determination. None of this would have been possible without you, I love you ma. Laura, thanks giving up many days and nights with me so I could work. Thanks for uprooting your life to move here with me and for being by my side for all this.

*For Murphy and Zeppy*

## Chapter 1

# Introduction to the Electronic Properties of Graphene

“Carbon is only the fifteenth most common element, accounting for a very modest 0.048 percent of the Earth’s crust, but we would be lost without it. What sets the carbon atom apart is that it is shamelessly promiscuous. It is the party animal of the atomic world, latching on to many other atoms (including itself) and holding tight, forming molecular conglomerates of hearty robustness - the very trick of nature necessary to build proteins and DNA.”<sup>1</sup>

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<sup>1</sup>Bill Bryson in *A Short History of Nearly Everything*, Broadway Books, Random House, p. 251.

## 1.1 Allotropes of carbon

Two allotropes of carbon are commonly used in daily life. The first, and perhaps better known, form is diamond. While very useful for a variety of purposes, diamond is a poor electrical conductor. This is a direct result of the bonding configuration of carbon atoms. In diamond, all of the  $p$ -orbitals of carbon are used in forming the bond, called  $sp^3$  bonding. As a result, there are no free electrons and conduction is poor. Graphite (from the Greek word to write) was discovered circa 1500 AD in England and was originally used to mark sheep. Graphite is a layered material comprised of many two-dimensional (2D) layers of carbon atoms arranged in a hexagonal lattice. While bonding in the 2D plane is strong, perpendicular to the plane it is weak. Graphite, unlike diamond, has only 2 of the 3  $p$  orbitals tied up in bonds. The one unpaired orbital, the  $p_z$  orbital, can be used in the transport of electrons. Hence, graphite is a much better conductor than diamond [1].

It is commonly thought that the next allotrope of carbon were fullerenes in the 1980's. However, a 2D version of graphite called graphene was first synthesized in the 1970's on the surface of metals. Using phase segregation of carbon-doped nickel single crystal, Eizenberg and Blakely [2] were able to controllably grow single layers of graphite. Originally, the potential of this material was mainly the ability to repel adsorbates from its surface (a phenomena discussed in Chapter 2) and it was thought that the nickel-single layer graphite system would find a use as a liner for the inside of ultra-high vacuum chambers.

Zero- and one-dimensional allotropes of carbon were discovered in the ensuing two decades. First were Buckminster Fullerenes, discovered in 1984 by Richard Smalley and coworkers [3]. Fullerenes are a ball of carbon atoms and can contain a few (20) to many (>1000) carbon atoms, with C60 being the first and most common in experiment. Carbon nanotubes are a one-dimensional wire of carbon atoms and were discovered by Ijima in the early 1990's [4]. Carbon nanotubes are still a very active area of research in physics, chemistry, biology and engineering.

The common feature to graphite, fullerenes and nanotubes is the hexagonal arrangement of carbon atoms. From a single sheet of hexagonal carbon atoms, all three of these allotropes can be obtained: the sheet can be stacked to form graphite, rolled into a tube to form a nanotube or bent into a ball to form a fullerene. It is only recently that the unique structural and electronic properties of a single layer of graphite, called graphene, have been widely appreciated. The electrical properties of a single sheet of graphene [5] on an insulating substrate were first measured about 100 miles from the place where graphite was discovered in Manchester, England and have since led to a dramatic increase in research in the field.

## 1.2 Band structure of graphene

The atomic layer of hexagonally arranged carbon atoms forming graphene is shown in Fig. 1.1(a). The unit cell [indicated by the dashed lines in Fig. 1.1(a)] is composed of two atoms, labeled A and B and has lattice vectors  $\vec{a}_1 = a(1, 0)$  and  $\vec{a}_2 = a(\frac{1}{2}, \frac{\sqrt{3}}{2})$ . The reciprocal lattice is also hexagonal, shown in Fig. 1.1(b) with the high symmetry points  $\Gamma$ , K and M.

The essential, low-energy features of the band structure can be captured by a tight-binding approximation. The eigenfunctions of graphene can be written as a linear combination of Bloch functions  $\phi_i(\vec{k}, \vec{r}) = \frac{1}{\sqrt{N}} \sum_{\vec{R}}^N e^{i\vec{k} \cdot \vec{R}} \chi_j(\vec{r} - \vec{R})$ , built up from the atomic wavefunctions  $\chi_j$  at site  $j$ , as

$$\Psi_i(\vec{k}, \vec{r}) = \sum_{i'=0}^n c_{ii'}(\vec{k}) \phi_i'(\vec{k}, \vec{r}). \quad (1.1)$$

The eigen-energies of this system can be obtained by

$$E_i(\vec{k}) = \frac{\langle \Psi_i | H | \Psi_i \rangle}{\langle \Psi_i | \Psi_i \rangle} = \frac{\sum_{jj'=0}^n c_{ij}^* c_{ij'} H_{jj'}(\vec{k})}{\sum_{jj'=0}^n c_{ij}^* c_{ij'} S_{jj'}(\vec{k})} \quad (1.2)$$

where  $H_{jj'}(\vec{k}) = \langle \Psi_j | H | \Psi_j' \rangle$  and  $S_{jj'}(\vec{k}) = \langle \Psi_j | \Psi_j' \rangle$ . The solution can be arrived at by minizing the above equation with respect to the coefficient  $c_{ij}^*$ , resulting in the secular

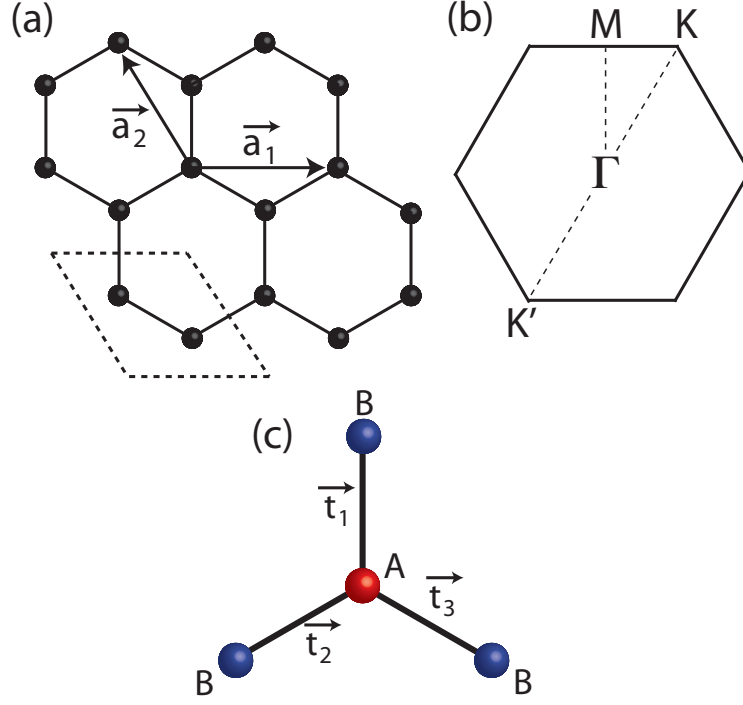


Figure 1.1: (a) Real space lattice of graphene. Unit cell vectors  $\vec{a}_1$  and  $\vec{a}_2$  designate the unit cell. The unit cell (indicated by the dashed lines) is composed of two atoms. (b) The reciprocal lattice and the high symmetry points  $\Gamma$ ,  $K$  and  $M$ . There are two inequivalent points in the Brillouin zone,  $K$  and  $K'$ . (c) Each  $A$  atom (red) is surrounded by 3 nearest neighbors  $B$  atoms (blue). Vectors  $\vec{t}_1$ ,  $\vec{t}_2$ , and  $\vec{t}_3$  connect the  $A$  atoms to the 3  $B$  atoms.

equation

$$\det[H - ES] = 0. \quad (1.3)$$

The simplest solution is obtained by considering only nearest neighbor interaction, thus only  $H_{AA}$ ,  $H_{BB}$ , and  $H_{AB}$ , where  $A$  and  $B$ , the two atoms of the graphene unit cell, need to be evaluated. Evaluation of energies  $H_{AA}$  and  $H_{BB}$  gives

$$H_{AA} = H_{BB} = \frac{1}{N} \sum_{\vec{R}, \vec{R}'} e^{i\vec{k}(\vec{R}-\vec{R}')} \langle \chi_A(\vec{r}-\vec{R}') | H | \chi_A(\vec{r}-\vec{R}) \rangle = \epsilon_{2p} \quad (1.4)$$

where  $\epsilon_{2p}$  is the orbital energy of the  $2p$  level. The off-diagonal elements  $H_{AB} = H_{BA}$  are calculated for the 3 nearest neighbor  $B$  atoms [see Fig. 1.1(c)] using the three vectors  $\vec{t}_1$ ,  $\vec{t}_2$  and  $\vec{t}_3$

$$H_{AB} = \gamma_H (e^{i\vec{k} \cdot \vec{t}_1} + e^{i\vec{k} \cdot \vec{t}_2} + e^{i\vec{k} \cdot \vec{t}_3}) = \gamma_h t(k) \quad (1.5)$$

$$S_{AB} = \gamma_S(e^{i\vec{k}\cdot\vec{t}_1} + e^{i\vec{k}\cdot\vec{t}_2} + e^{i\vec{k}\cdot\vec{t}_3}) = \gamma_S t(k) \quad (1.6)$$

where  $\gamma_h = \langle \chi_A(\vec{r} - \vec{R}') | H | \chi_B(\vec{r} - \vec{R} + \vec{t}) \rangle$  and  $\gamma_s = \langle \chi_A(\vec{r} - \vec{R}') | \chi_B(\vec{r} - \vec{R} + \vec{t}) \rangle$ . The determinants for  $H$  and  $S$  are then

$$H = \begin{pmatrix} \epsilon_{2p} & \gamma_h t(k) \\ \gamma_h t(k) & \epsilon_{2p} \end{pmatrix}$$

$$S = \begin{pmatrix} 1 & \gamma_s t(k) \\ \gamma_s t(k) & 1 \end{pmatrix}.$$

Using these two matrices, the solution to the secular equation 1.3 is

$$E(\vec{k}) = \frac{\epsilon_{2p} \pm \gamma_h u(\vec{k})}{1 \pm \gamma_s u(\vec{k})} \quad (1.7)$$

$$u(\vec{k}) = \sqrt{1 + 4 \cos \frac{\sqrt{3}k_y a}{2} \cos \frac{k_x a}{2} + 4 \cos^2 \frac{k_x a}{2}}. \quad (1.8)$$

The resulting band structure is shown in Fig. 1.2 using the parameters  $\epsilon_{2p}=0$ ,  $\gamma_h=-3\text{eV}$  and  $\gamma_s=0.129$  [1]. Note that the energy dispersion curves for  $E>0$  meet the curves for  $E<0$  at the K points in the Brillouin zone. For small  $\vec{k}$  values around these K points, the energy  $E$  is *linear* in  $\vec{k}$ . It is this low-energy, linear relationship that gives graphene its unique electronic properties.

### 1.3 Quantum Hall effect in graphene

Discovered 29 years ago, the quantum Hall effect illustrated new physics that can be observed in systems confined to two dimensions [6]. Since graphene is an ultra-2D system (it is only one atom thick), it is natural to ask what the quantum Hall effect looks like in this system. The underlying band structure of graphene produces quantum Hall conductance values different from conventional semiconducting 2D materials [7].

The low-energy Hamiltonian for graphene is equivalent to that of massless Dirac fermions [8]. In the presence of a magnetic field, the Hamiltonian is altered using a Peirels substitution

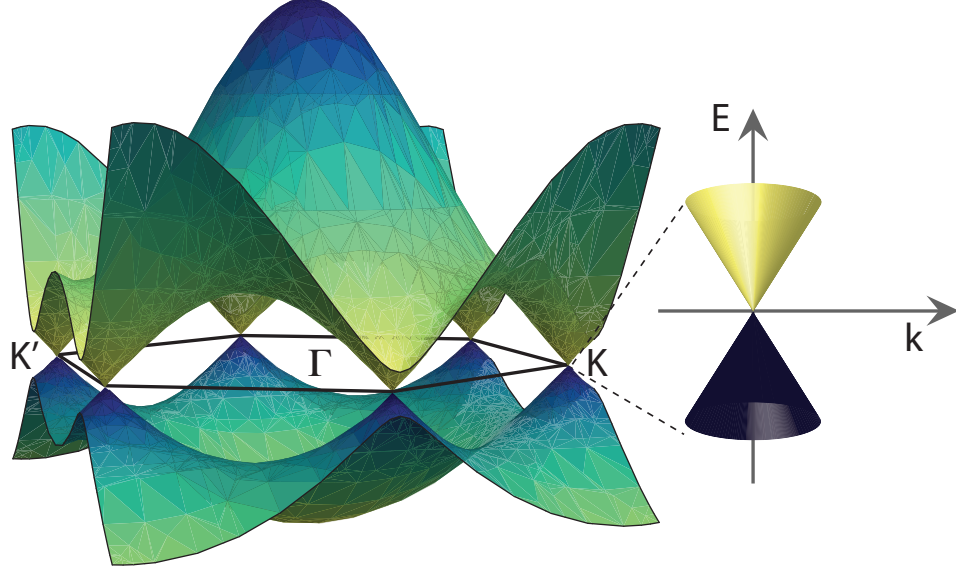


Figure 1.2: Electronic band structure of graphene, obtained using a tight-binding approximation for nearest neighbor hopping only. For small values of wavevector  $\vec{k}$  around the K and K' points, the energy  $E$  is linear in  $\vec{k}$ .

$(\vec{p} \rightarrow \vec{p} + e\vec{A})$ , resulting in

$$-v_F(\vec{p} + e\vec{A}) \cdot \sigma \psi(\vec{r}) = E\psi(\vec{r}) \quad (1.9)$$

where  $v_F$  is the Fermi velocity ( $v_F \sim 10^6 \text{ m}^2$ ),  $\sigma$  are the Pauli matrices and  $\psi(\vec{r})$  is a two component wavefunction. Working in the Landau gauge ( $\vec{A} = -By\hat{x}$ ), the first component of the wavefunction  $\psi_1$  can be eliminated to give

$$v_F^2(p^2 - 2eBy p_x - e^2 B^2 y^2 - \hbar e B)\psi_2(\vec{r}) = E^2 \psi_2(\vec{r}). \quad (1.10)$$

This equation can be solved to find the eigen-energies of the Landau levels (LL)

$$E_n = \sqrt{2e\hbar v_F^2 |n| B} \quad (1.11)$$

for  $|n|=0,1,2,\dots$ . Equation 1.11 can be compared to the dispersion obtained for conventional 2D materials [6], where  $E_n = \hbar\omega_c(n + 1/2)$ . The first difference is that in Eq. 1.11, there is a LL at zero energy (for  $|n| = 0$ ), where in conventional 2D case, the LL energy is always  $\geq \hbar\omega_c/2$ . This zero-energy LL is comprised on equal parts of electron and holes (see Fig.

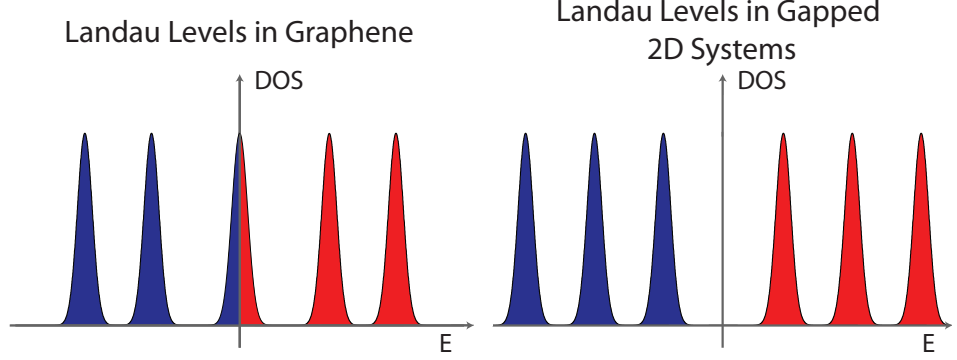


Figure 1.3: Landau levels in graphene (left) and in conventional 2D materials (right). The two main differences are the presence of a zero-energy Landau level and the  $\sqrt{n}$  spacing of the levels in graphene.

1.3), a demand of particle-hole symmetry in graphene. As carriers in the zero-energy LL approach the edge of the sample, the energy of the electron-like excitations is increased while the energy for the hole-like excitations decreases. This “splitting” of the zero-energy LL results in the first edge state above  $E=0$  to have half the degeneracy of the of the remaining LL, giving rise to the “half-integer” quantum Hall effect observed experimentally [9, 10] and predicted theoretically [11, 12]. The quantized transverse conductivity values occur at

$$\sigma_{xy} = 4(n + 1/2) e^2/h = 2, 6, 10, \dots e^2/h \quad (1.12)$$

different from conventional 2D materials [6] and from 2 layers of graphene [13]. Consequently, this unique conductance quantization provides a useful method for distinguishing one graphene layer from two. The second important difference between conventional 2D materials is that in Eq. 1.11 the energy levels are spaced as  $\sqrt{n}$ , resulting in relatively more closely-spaced LL at higher energies in graphene. These two differences are summarized in Fig. 1.3.

## 1.4 Potential barriers in graphene

In the last section, the difference between graphene and other 2D materials was demonstrated at large magnetic fields. In addition, the linear energy dispersion in graphene results

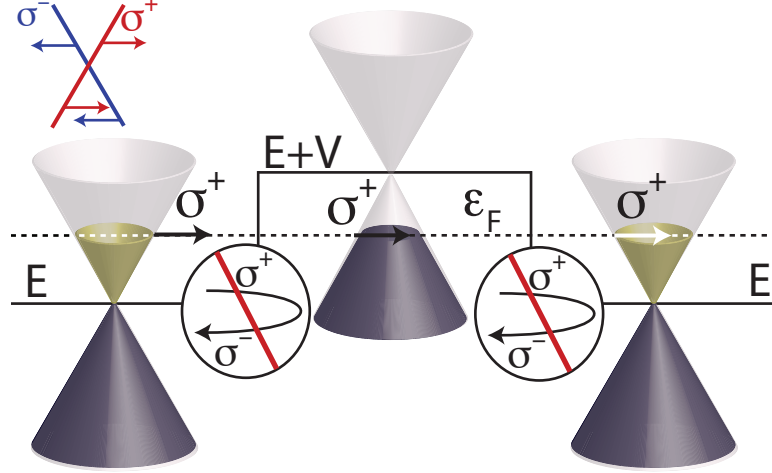


Figure 1.4: In graphene, pseudospin is linked with direction of propagation (inset in upper left corner). For pseudospin-preserving barriers and for motion perpendicular to the barrier, turning around is prohibited and the transmission through the barrier is unity. The effect is known as the Klein paradox.

in differences at zero magnetic field. There are a number of ways to create potential barriers in 2D materials. Traditionally it is done via the electric-field effect [14] and focus is given to this method as it is the sole technique used in the experiments of this thesis. For gapped materials, an electric field can either switch “off” the current (field-effect transistor) or can result in rectifying behavior ( $p$ - $n$  diode). Graphene is a gapless system, so the “off” state is not achievable (for creating a gap in graphene so that an “off” state is possible, see the section below on nanoribbons). Rectification in  $p$ - $n$  junctions is a result of a depletion region — a by-product of a gapped system — hence graphene  $p$ - $n$  junctions cannot rectify.

It was recognized 80 years ago that the solution to a step potential [ $H(x - a/2) - H(x + a/2)$ ], where  $H$  is the Heavyside function and  $a$  is the length of the potential step] for the Dirac equation was very different from the solution for the same potential in the Schrödinger equation [15]. Unlike the Schrödinger equation, where transmission through the barrier is exponentially suppressed with increased height and width, Klein demonstrated that for Dirac carriers with rest energy  $\Delta = 2mc^2$  approaching the barrier at normal incidence had unity transmission, for barrier heights  $V > \Delta$ . This effect, which now bears the author’s name, is called the “Klein Paradox”. In graphene the carriers lack mass and it is expected

that unity transmission will occur for all values of  $V$ . One explanation for this effect can be understood by the lack of the band gap in the eigen-energies of the Dirac equation. This leads to a vanishing distance between classical turning points [16] outside and inside the barrier. Another interpretation comes from the pseudospin concept of carriers in graphene. The wavefunction of Eq. 1.9 is a two-component wavefunction, each component coming from the amplitude of the wavefunction on sublattice A and B. It can be shown [17] that the right movers (those states with  $\delta E/\delta k > 0$ , shown in red in the inset of Fig. 1.4), come from the A atoms and the left movers ( $\delta E/\delta k < 0$ , blue in the inset of Fig. 1.4) come from the B atoms. The Pauli matrices of Eq. 1.9 affect the amplitude of the wavefunction on the A and B atoms and are not operating on the electron spin. As such it has become conventional to associate  $\sigma$  with the “spin-like” properties of the amplitude on the two sublattices called pseudospin. In a single valley (when K-K’ scattering is small, i.e. for potential steps that vary slowly on the scale of the lattice constant  $a$ ), to change from a right mover to a left mover requires a flip of pseudospin, which is prohibited if the barrier is pseudospin conserving. This pseudospin conservation prevents the particle from turning around anywhere in the barrier (Fig. 1.4) and the transmission is unity.

## 1.5 Graphene nanoribbons

As mentioned in the previous section, graphene cannot be put in an “off” state due to lack of a band gap, making it useless for creating transistors with large on-off ratios. Like in carbon nanotubes, reducing the dimensions of graphene one further to produce one-dimensional graphene wires called nanoribbons, can induce a gap. Nanoribbons can be terminated in two separate ways called zig-zag or arm chair, and this termination along with the width of the ribbon dictate the size of the band gap [18]. In a nanoribbon, the states perpendicular to the ribbon direction are quantized, resulting in a few allowed, boundary-condition-defined k-vectors. Where these allowed k-vectors cut through the Brillouin zone

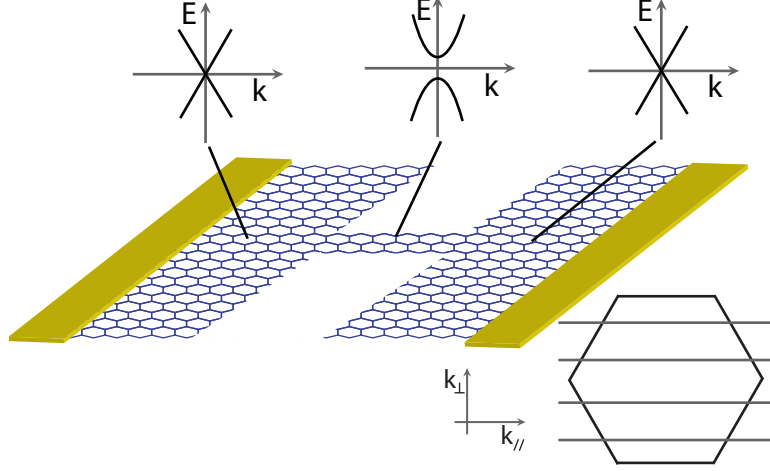


Figure 1.5: By forming a one-dimensional wire in graphene, producing a graphene nanoribbon, the gapless band structure can be altered and can become gapped. Introducing confinement in one more dimension produces on a few allowed perpendicular wave vectors that cut through the Dirac cones resulting in the band gap in the constriction.

(lower left inset of Fig. 1.5) determine if there is a gap and the size of the separation in energy of the valence and conduction bands [1]. A graphene nanoribbon transistor schematic is shown in Fig. 1.5.

The ability to control the gap from a top-down approach (i.e. etching away 2D graphene) is a distinct advantage over carbon nanotubes, where semiconducting and metallic tubes can be grown, but in unpredictable way. This top-down method requires precise control, at the atomic level, over the width and edge termination of the nanoribbon. Nanoribbons have been created synthetically [19, 20] and by oxygen plasma etching [21, 22], however the precise control of the edge termination remains an experimental challenge.

## 1.6 Minimum conductivity in graphene

In 2D semiconductors, the conductivity is related to the density of electronic states [14]

$$\sigma = e^2 \rho(E_F) D. \quad (1.13)$$

Exactly at the K and K' points, the density of states vanishes. When the Fermi level is at these points (called the Dirac points), Eq. 1.13 expected to be zero. However, a

quantum treatment results in a finite conductivity at the Dirac point [23, 24], a result of the underlying inability to localize Dirac electrons in 2D. For a clean system of graphene, the expected minimum conductivity is  $4/\pi e^2/h$  [25].

In real graphene devices, disorder plays an important role in charge transport [26]. Three main types of disorder are possible: dislocations, ripples and charged impurity scattering. Scanning tunneling microscopy studies have shown that the amount of dislocations in exfoliated graphene is small [27]. Ripples are slow, smooth variations of the graphene height and can arise from corrugations of the surface [28] or intrinsically from long-wavelength fluctuations of the graphene membrane [29]. The last main source of disorder is charge impurities, either from the SiO<sub>2</sub> substrate or from charges trapped beneath or lying on top of the graphene sheet [30]. It is currently unclear whether ripples [31] or charge impurities [32] are the more important factor in determining the conductivity in graphene. It is known that at the Dirac point disorder produces a series of interconnected puddles of electrons and holes [33]. Therefore, it is not possible to define a  $E_F$  where the energy is positioned exactly at the Dirac point. Instead, a value of  $E_F$  can be assigned such that the entire sheet of graphene is charge neutral: this point is called the charge-neutrality point. The minimum conductivity at the charge-neutrality point has been studied experimentally [13, 34] and theoretically [35, 36], though no consensus has been reached. It is important to point out that since the charge neutrality point is made up entirely of  $p$ - $n$  puddles and  $p$ - $n$  junctions, understanding how carriers move through this environment is critical to having a clear picture of what the minimum conductivity should be in graphene.

## Chapter 2

# Functionalization of and Atomic Layer Deposition on Graphene

## 2.1 Atomic Layer Deposition

Atomic Layer Deposition (ALD) is a process by which metals and multi-component oxides can be grown layer by layer. In particular, high quality, high- $\kappa$  materials like  $\text{Al}_2\text{O}_3$  and  $\text{HfO}_2$  can be grown via ALD. A resurgence of interest in this method has occurred in the last decade due to the need for high- $\kappa$  dielectrics in silicon-based transistors. For example, Intel recently began using  $\text{Al}_2\text{O}_3$  grown by ALD as the gate dielectric in their 45nm technology. A great review of the ALD process and its applications can be found in Ref. [37].

While the creation of designer precursor chemicals and the understanding of the surface chemistry of these precursors are difficult, the idea behind ALD is relatively simple. First, a substrate is placed in an evacuated chamber where the ALD growth will occur. Then, a fixed amount of a precursor gas [Precursor 1 in Fig. 2.1(a)] is pulsed into the ALD chamber. This precursor chemically reacts with the substrate surface and binds to the surface. For the reaction to occur, only specific sites [indicated by the triangular shapes in the substrate in Fig. 2.1(a)] on the surface must be catalytically suitable for this reaction to occur: if the precursor cannot find these sites, the reaction cannot start and the precursor is pumped out of the chamber. Once all the catalytic sites are occupied, further reactions are not permitted making this process self-limited to adsorption of a single monolayer of the precursor ([Fig. 2.1(b)]. After enough precursor 1 is introduced into the chamber to fill all the sites, a second precursor is pulsed into the chamber. Here, it is precursor 1 that provides the catalytic sites for precursor 2 to chemically adsorb on the surface. Again, this process is self-limiting, terminating when all the sites of the precursor 1 layer are occupied. By repeating this process, oxides can be built up a single atomic layer at a time with a high degree of uniformity and oxide quality.

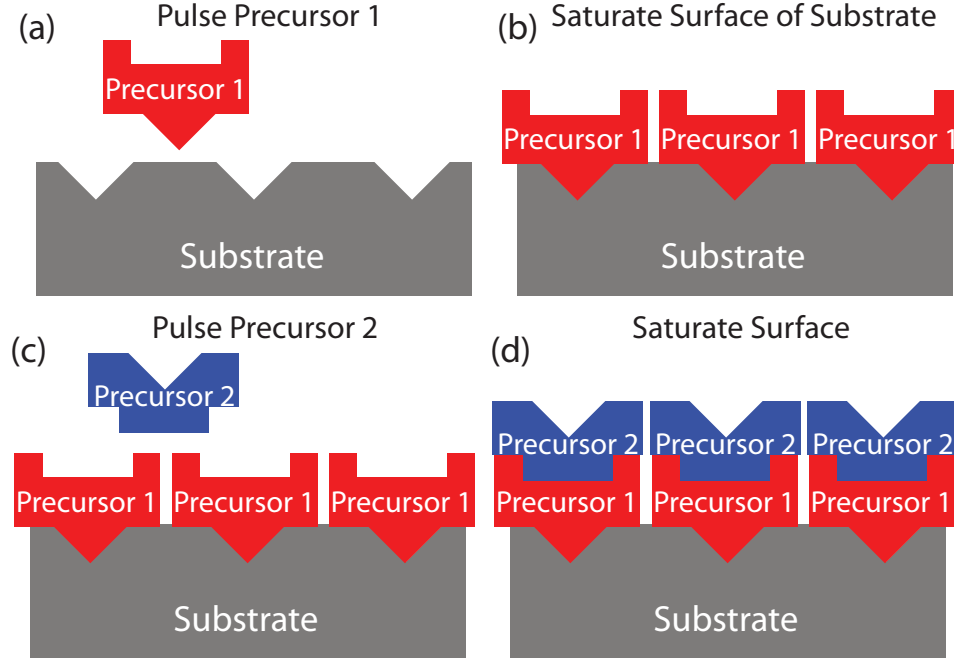


Figure 2.1: Schematic of the Atomic Layer Deposition Process. (a) Precursor 1 is introduced into the ALD chamber. (b) Precursor 1 chemically reacts with the surface at specific sites (indicated by triangles) and adsorbs on the surface. This process is self-limiting and ceases after all the sites on the substrate surface are occupied. (c) A second precursor, Precursor 2, is introduced into the chamber. (d) Precursor 1 provides the catalytic sites for Precursor 2 to adsorb. This process is also self-limiting. By repeating this cycle, oxides can be built up layer by layer.

## 2.2 Atomic Layer Deposition on graphene

To achieve local control of carrier type and density in graphene via the electric field effect a local gate, insulated from the graphene device, must be fabricated. It is trivial to place a metallic gate electrode in close proximity to a sheet of graphene. It is not as trivial to insulate that gate from the device. Here, I will describe a method for producing a gate dielectric that preserves the unique properties of graphene and was an *essential* experimental step in obtaining the results of Chapters 2, 3 and 6.

$\text{Al}_2\text{O}_3$  is grown via ALD by successive deposition of trimethylaluminum (TMA) and water. Many attempts were made to deposit  $\text{Al}_2\text{O}_3$  on graphene by varying temperature, deposition amount and pump time. However, most (95%) devices had top gates that leaked, that is, when a voltage was applied to the top gate, a current was measured proportional to

that voltage in the device. The few devices that did not leak had very thin top gates and resulted in heavily electron-doped graphene, with a charge-neutrality point of  $\lesssim -30\text{V}$ . Those that did leak had a leakage resistance of roughly  $1\text{k}\Omega$ , a value close to the resistance of the graphene-Ti/Au interface (contact resistance), suggesting that most of the top gate was in electric contact with the graphene sheet. It was since discovered that on pristine graphene, the ALD precursors preferentially nucleate at edges and defect sites, not on the pristine graphene plane, resulting in a discontinuous film [38]. In fact, a similar phenomena was observed a year prior in carbon nanotubes [39] and it was found that a functionalization layer (FL) was needed to pretreat the surface of the nanotube before it was suitable for ALD growth of oxide.

The Marcus Lab has one of the first ALD machines created by a former Marcus Lab postdoc, Douwe Monsma, and former Prof. Gordon Lab graduate student, Jill Becker. The Cambridge Nanotech ([www.cambridgenanotech.com](http://www.cambridgenanotech.com)) Savannah 100 is shown in Fig. 2.2, and the details of the system can be found at the company website. Briefly, the system consists the following components: a gas cabinet that houses the ALD precursors and the  $\text{NO}_2$  used in the functionalization layer, a reaction chamber where the precursor gases interact with the sample and a control computer. Not shown is the wet pump (Leybold Trivac 016B) behind the wall. The length of KF-25 bellow connecting the reaction chamber to the pump is 3'. The base pressure of this setup is 0.4 torr with 20 sccm of  $\text{N}_2$  flowing into the reaction chamber.

### 2.3 $\text{NO}_2$ and gas cabinet modification

A similar pretreatment is necessary for graphene, and an approach similar to that for nanotubes [39] was undertaken. The main ingredient of the FL is  $\text{NO}_2$ . A small lecture bottle of liquid dinitrogen tetroxide (Fig. 2.2) was purchased from Matheson TriGas. Dinitrogen tetroxide is a liquid that evaporates into  $\text{NO}_2$  and has a vapor pressure at room



Figure 2.2: The Savannah 100 by Cambridge Nanotech.

temperature of about an atmosphere.

The dinitrogen tetroxide bottle was mounted on the side of the gas cabinet. 1/4"

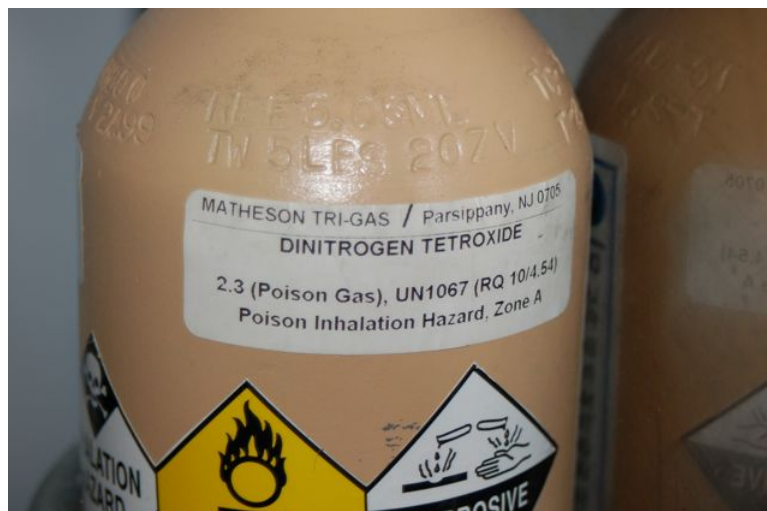


Figure 2.3: 1 liter lecture bottle of dinitrogen tetroxide obtained from Matheson TriGas.

stainless steel tubing was attached to the lecture bottle and runs up the Parker solenoid valve. The total volume of the tube is  $3.5 \text{ in}^3$ . No regulator is required as the vapor pressure is low. Initially, the water precursor value was split into two lines and the water precursor was fed into one line and the  $\text{NO}_2$  into the other. Over time I have found that water and/or  $\text{NO}_2$  collects in the piping and at some point forms nitric acid and bubbles into the reaction chamber. Now, only one line goes to the solenoid valve and when switching is needed between water and  $\text{NO}_2$ , one line is disconnected and the other is attached. Ideally, a fixed line going to the chamber that never sees atmosphere would go to the chamber but this is not possible, as the Savannah 100 has only two (for the older models) or 1 (for the newer models) port to the reaction chamber. To accommodate the safety concerns of having  $\text{NO}_2$  in the lab, the gas cabinet was completely closed and a pipe was mounted on the back panel on the cabinet (see inset of Fig. 2.3) and connected to house vacuum. The present gas cabinet is shown in Fig. 2.3.

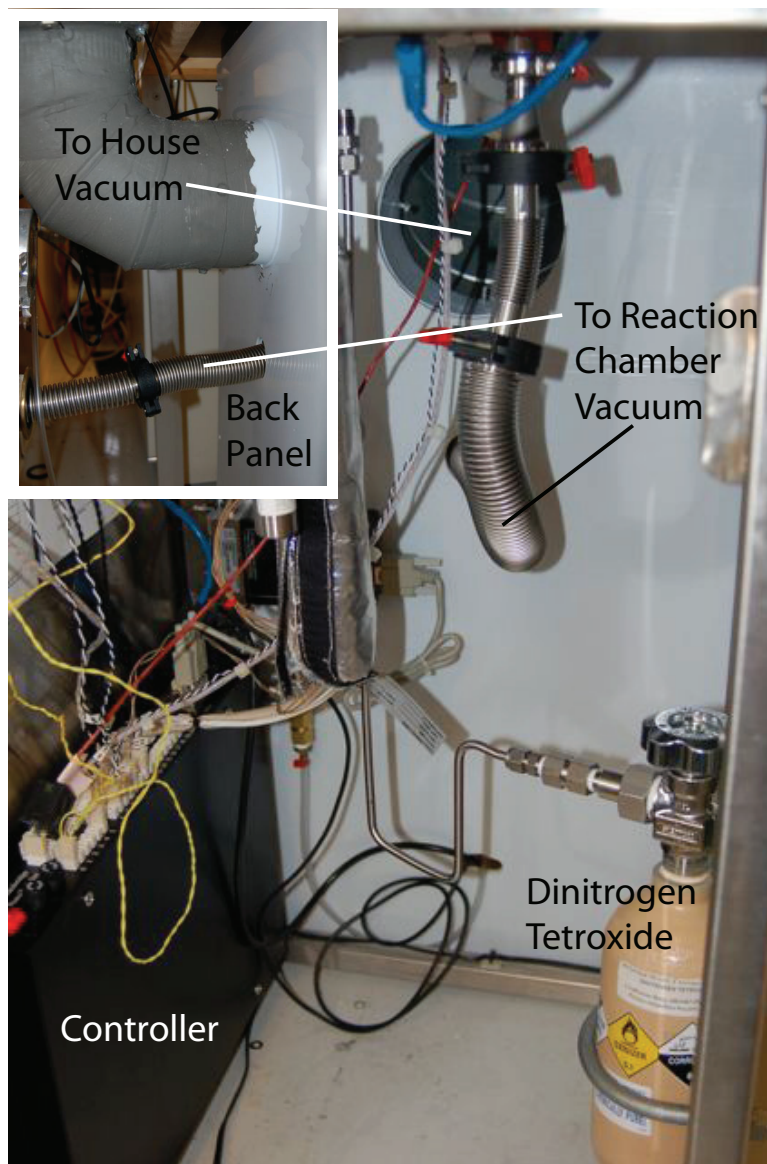


Figure 2.4: The standard gas cabinet has been modified to accomodate the  $\text{NO}_2$  lecture bottle.

## 2.4 Deposition of the functionalization layer

The surface of graphene is catalytically unsuitable for the formation of oxide using precursors TMA and water. Before deposition of a top gate oxide, the surface of graphene must be pretreated with a functionalization layer (FL) that ideally would accomplish three functions: the FL should not affect the unique electronic properties of graphene, it should chemically dope the graphene and should leave behind a surface that is catalytically suitable

for subsequent oxide growth via ALD. To this end, a FL comprised of successive pulses of  $\text{NO}_2$  (g) and TMA (g) are deposited at room temperature ( $\sim 30^\circ\text{C}$ ) on the entire chip containing a graphene sheet with electrical contacts.

Before the chip is placed in the reaction chamber, the  $\text{NO}_2$  and TMA lines are attached to the Parker solenoid valves with a stainless steel VCR gasket. The lines are then evacuated by running the recipe Purging the Lines (Table 2.1), repeating the two step process 10 times. The pressure in each line should fall to the chamber pressure within a few pulses.

Table 2.1: Purging the Lines

Line	Pulse Time (sec)	Pump Time (sec)
$\text{NO}_2$	0.1	10
TMA	0.1	10

First, the chip is placed in the reaction chamber at  $160^\circ\text{C}$ . Once the chip is in the chamber, the heaters to the chamber are turned off and allowed it to cool to room temperature. This should take about 4 hours. This step is like an anneal in an  $\text{N}_2$  background. Water tapped under the FL and graphene at room temperature expands as the temperature is increased (for the oxide deposition) and causes bubbling of the graphene device. Once the temperature of the chamber reaches  $\sim 30^\circ\text{C}$ , the deposition of the FL can begin. The FL is deposited repeating the Functionalization Recipe in Table 2.2 nine times.

Table 2.2: Functionalization Recipe

Line	Pulse Time (sec)	Pump Time (sec)
$\text{NO}_2$	0.3	7
TMA	0.1	5
TMA	0.1	5
TMA	0.1	120

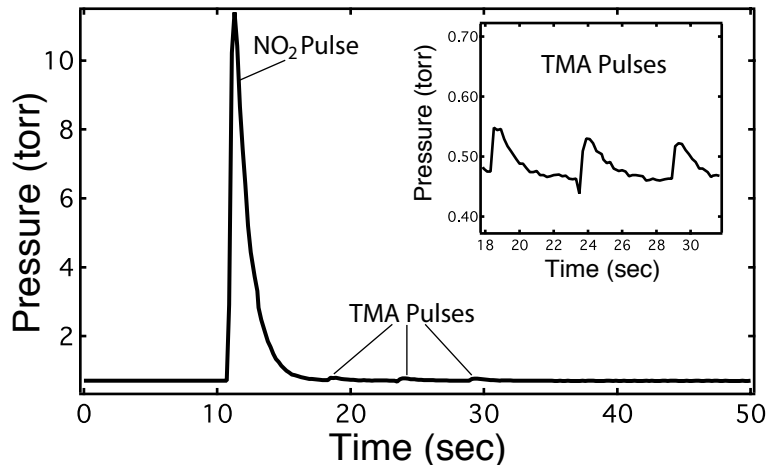


Figure 2.5: Pulse heights for one step of the Functionalization Recipe. A large  $\text{NO}_2$  pulse is followed by three smaller pulses of TMA. The inset shows a zoom in of the three TMA pulses.

It is important to perform the extra TMA pulses. There is a critical pressure magnitude of the  $\text{NO}_2$  pulse and a critical ratio between the  $\text{NO}_2$  and TMA. If the  $\text{NO}_2$  pulse is too small, then the functionalization layer will not fully cover the graphene sheet and the device will leak. If the ratio is not correct, the graphene sheet will be doped and the mobility will be very poor ( $\sim 100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-2}$ ). A typical pulse sequence is shown in Fig. 2.4.

## 2.5 Deposition of $\text{Al}_2\text{O}_3$

After performing the nine repetitions of the Functionalization recipe, the  $\text{NO}_2$  line from the 1<sup>st</sup> solenoid valve is removed and the water line is attached. A heater jacket is placed around the water canister and the temperature is set to  $40^\circ\text{C}$ . Before raising the temperature, 5 cycles of a standard ALD process at room temperature is performed to prevent desorption of the FL. 5 cycles of the recipe in Table 2.3, Stabilizing the FL.

Finally, the temperature of the reaction chamber can be raised to perform the oxide growth. The temperature of the base of the reaction chamber is set to  $160^\circ\text{C}$  and the walls of the chamber to  $150^\circ\text{C}$ . Wait until the chamber has reached its set temperature ( $\sim 5$  mins) and perform the Oxide Growth recipe in Table 2.4. Repeat the process to suit the

Table 2.3: Stabilizing the FL

Line	Pulse Time (sec)	Pump Time (sec)
H <sub>2</sub> O	0.2	5
TMA	0.1	30

Table 2.4: Oxide Growth

Line	Pulse Time (sec)	Pump Time (sec)
H <sub>2</sub> O	0.2	5
TMA	0.1	30

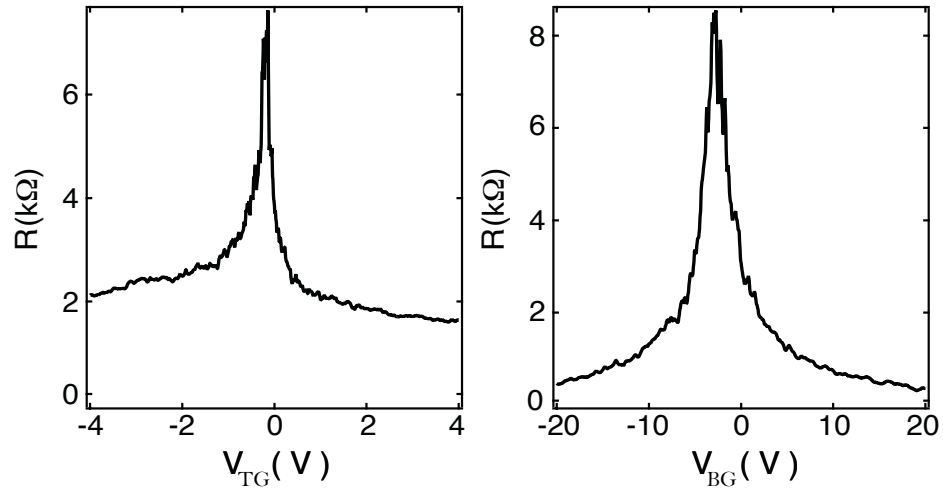


Figure 2.6: Two-terminal resistance  $R$  as a function of  $V_{tg}$  (left) and  $V_{bg}$  (right) after deposition of the functionalization layer and 30 nm of  $Al_2O_3$

desired oxide thickness, each cycle deposits about 0.09 nm.

If done properly, the mobility of the graphene should be very close to the mobility before deposition and the charge-neutrality point should be around zero. Fig. 2.5 shows the results for a device with  $\sim 10,000$ ,  $cm^2 V^{-1} s^{-2}$  mobility.

## Chapter 3

# Quantum Hall effect in a gate-controlled $p$ - $n$ junction in graphene

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The unique band structure of graphene allows reconfigurable electric-field control of carrier type and density, making graphene an ideal candidate for bipolar nanoelectronics. We report the realization of a single-layer graphene  $p$ - $n$  junction in which carrier type and density in two adjacent regions are locally controlled by electrostatic gating. Transport measurements in the quantum Hall regime reveal new plateaus of two-terminal conductance across the junction at 1 and  $3/2$  times the quantum of conductance,  $e^2/h$ , consistent with recent theory. Beyond enabling investigations in condensed matter physics, the local-gating technique demonstrated here sets the foundation for a future graphene-based bipolar technology.<sup>1 2</sup>

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<sup>1</sup>This chapter is adapted with permission from Science **317**, 638 (2007). © (2007) by the American Association for the Advancement of Science.

<sup>2</sup>This chapter is adapted from Ref. [40].

### 3.1 Introduction

Graphene, a single-layer hexagonal lattice of carbon atoms, has recently emerged as a fascinating system for fundamental studies in condensed matter physics [7], as well as a candidate for novel sensors [41, 42] and post-silicon electronics [5, 21, 22, 43, 44, 46, 47]. The unusual band structure of single-layer graphene makes it a zero-gap semiconductor with a linear (photon-like) energy-momentum relation near the points where valence and conduction bands meet. Carrier type—electron-like or hole-like—and density can be controlled using the electric-field effect [5], obviating conventional semiconductor doping, for instance via ion implantation. This feature, doping via local gates, would allow graphene-based bipolar technology—devices comprising junctions between hole-like and electron-like regions, or  $p$ - $n$  junctions—to be reconfigurable, using only gate voltages to distinguish  $p$  (hole-like) and  $n$  (electron-like) regions within a single sheet. While global control of carrier type and density in graphene using a single back gate has been investigated by several groups [9, 10, 45], local control [46, 47] of single-layer graphene has remained an important technological milestone. In addition,  $p$ - $n$  junctions are of great interest for low-dimensional condensed matter physics. For instance, recent theory predicts that a local step in potential would allow solid-state realizations of relativistic (“Klein”) tunneling [17, 16], and a surprising scattering effect known as Veselago lensing [48], comparable to scattering of electromagnetic waves in negative-index materials [49].

We report the realization of local top gating in a single-layer graphene device which, combined with global back gating, allows individual control of carrier type and density in adjacent regions of a single atomic layer. Transport measurements at zero perpendicular magnetic field  $B_{\perp}$  and in the quantum Hall (QH) regime demonstrate that the functionalized aluminum oxide ( $\text{Al}_2\text{O}_3$ ) separating the graphene from the top gate does not significantly dope the layer nor affect its low-frequency transport properties. We study the QH signature of the graphene  $p$ - $n$  junction, finding new conductance plateaus at 1 and  $3/2 e^2/h$ , consistent

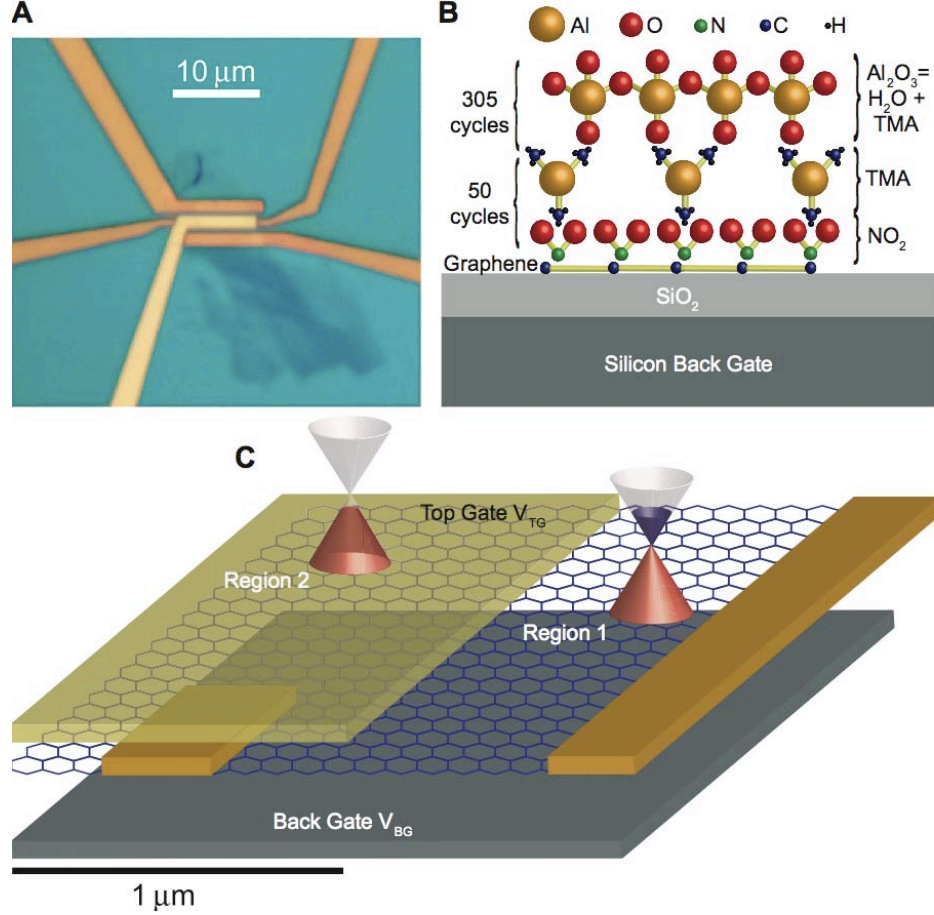


Figure 3.1: (a) Optical micrograph of a device similar to the one measured. Metallic contacts and top gate appear in orange and yellow, respectively. Darker regions below the contacts are thicker graphite from which the contacted single layer of graphene extends. (b) Illustration of the oxide deposition process. A non-covalent functionalization layer is first deposited using NO<sub>2</sub> and TMA (50 cycles) and Al<sub>2</sub>O<sub>3</sub> is then grown by atomic layer deposition using H<sub>2</sub>O-TMA (305 cycles yielding ~ 30 nm thickness). (c) Schematic diagram of the device measured in this experiment.

with recent theory addressing equilibration of edge states at the  $p$ - $n$  interface [50].

### 3.2 Device fabrication

Graphene sheets are prepared via mechanical exfoliation using a method similar to that used in Ref. [5]. Graphite flakes are deposited on 300 nm of SiO<sub>2</sub> on a degenerately doped Si substrate. Inspection with an optical microscope allows potential single-layer regions of graphene to be identified by a characteristic coloration that arises from thin-film

interference. These micron-scale regions are contacted with thermally evaporated Ti/Au (5/40 nm), and patterned using electron-beam lithography. Next, a  $\sim 30$  nm layer of oxide is deposited atop the entire substrate. As illustrated [Fig. 3.1(b)], the oxide consists of two parts: a non-covalent functionalization layer (NCFL) and  $\text{Al}_2\text{O}_3$ . This deposition technique is based on a recipe successfully applied to carbon nanotubes [39]. The NCFL serves two purposes. One is to create a non-interacting layer between the graphene and the  $\text{Al}_2\text{O}_3$  and the other is to obtain a layer that is catalytically suitable for the formation of  $\text{Al}_2\text{O}_3$  by atomic layer deposition (ALD). The NCFL is synthesized by 50 pulsed cycles of  $\text{NO}_2$  and trimethylaluminum (TMA) at room temperature inside an ALD reactor. Next, 5 cycles of  $\text{H}_2\text{O}$ -TMA are applied at room temperature to prevent desorption of the NCFL. Finally,  $\text{Al}_2\text{O}_3$  is grown at  $225^\circ\text{C}$  with 300  $\text{H}_2\text{O}$ -TMA ALD cycles. To complete the device, a second step of electron-beam lithography defines a local top gate (5/40 nm Ti/Au) covering a region of the device that includes one of the metallic contacts.

### 3.3 Measurement setup

A completed device, similar in design to that shown in the optical image in Fig. 3.1(a), was cooled in a  $^3\text{He}$  refrigerator and characterized at temperatures  $T$  of 250 mK and 4.2 K. Differential resistance  $R = dV/dI$ , where  $I$  is the current and  $V$  the source-drain voltage, was measured by standard lock-in techniques with a current bias of 1 (10)  $\text{nA}_{\text{rms}}$  at 95 Hz for  $T = 250$  mK (4.2 K). The voltage across two contacts on the device, one outside the top-gate region and one underneath the top gate, was measured in a four-wire configuration, eliminating series resistance of the cryostat lines. A schematic of the device is shown in Fig. 3.1(c).

### 3.4 Transport at zero magnetic field

The differential resistance  $R$  as a function of back-gate voltage  $V_{\text{bg}}$  and top-gate voltage  $V_{\text{tg}}$  at  $B_{\perp} = 0$  [Fig. 3.2(a)], demonstrates independent control of carrier type and density in the two regions. This two-dimensional (2D) plot reveals a skewed, cross-like pattern that separates the space of top-gate and back-gate voltages into four quadrants of well-defined carrier type in the two regions of the sample. The horizontal (diagonal) ridge corresponds to charge neutrality, i.e., the Dirac point, in region 1 (2). The slope of the charge-neutral line in region 2, along with the known distances to the top gate and back gate, gives a dielectric constant  $\kappa \sim 6$  for the functionalized  $\text{Al}_2\text{O}_3$ . The center of the cross at  $(V_{\text{tg}}, V_{\text{bg}}) \sim (-0.2 \text{ V}, -2.5 \text{ V})$  corresponds to charge neutrality across the entire graphene sample. Its proximity to the origin of gate voltages demonstrates that the functionalized oxide does not chemically dope the graphene significantly.

Slices through the 2D conductance plot at fixed  $V_{\text{tg}}$  are shown in Fig. 3.2(c). The slice at  $V_{\text{tg}} = 0$  shows a single peak commonly observed in devices with only a global back gate [5, 9, 10, 45]. Using a Drude model away from the charge-neutrality region, mobility is estimated at  $\sim 7000 \text{ cm}^2/\text{Vs}$  [5]. The peak width, height, and back-gate position are consistent with single-layer graphene [9, 10, 45] and provides evidence that the electronic structure and degree of disorder of the graphene is not strongly affected by the oxide. Slices at finite  $|V_{\text{tg}}|$  reveal a doubly-peaked structure. The weaker peak, which remains near  $V_{\text{bg}} \sim -2.5 \text{ V}$  at all  $V_{\text{tg}}$ , corresponds to the Dirac point of region 1. The stronger peak, which moves linearly with  $V_{\text{tg}}$ , is the Dirac point for region 2. The difference in peak heights is a consequence of the different aspect ratios of regions 1 and 2. Horizontal slices at fixed  $V_{\text{bg}}$  corresponding to the horizontal lines in Fig. 3.2(a) are shown in Fig. 3.2(b). These slices show a single peak corresponding to the Dirac point of region 2. This peak becomes asymmetric away from the charge-neutrality point in region 1. We note that the  $V_{\text{bg}}$  dependence of the asymmetry is opposite to that observed in Ref. [47], where the

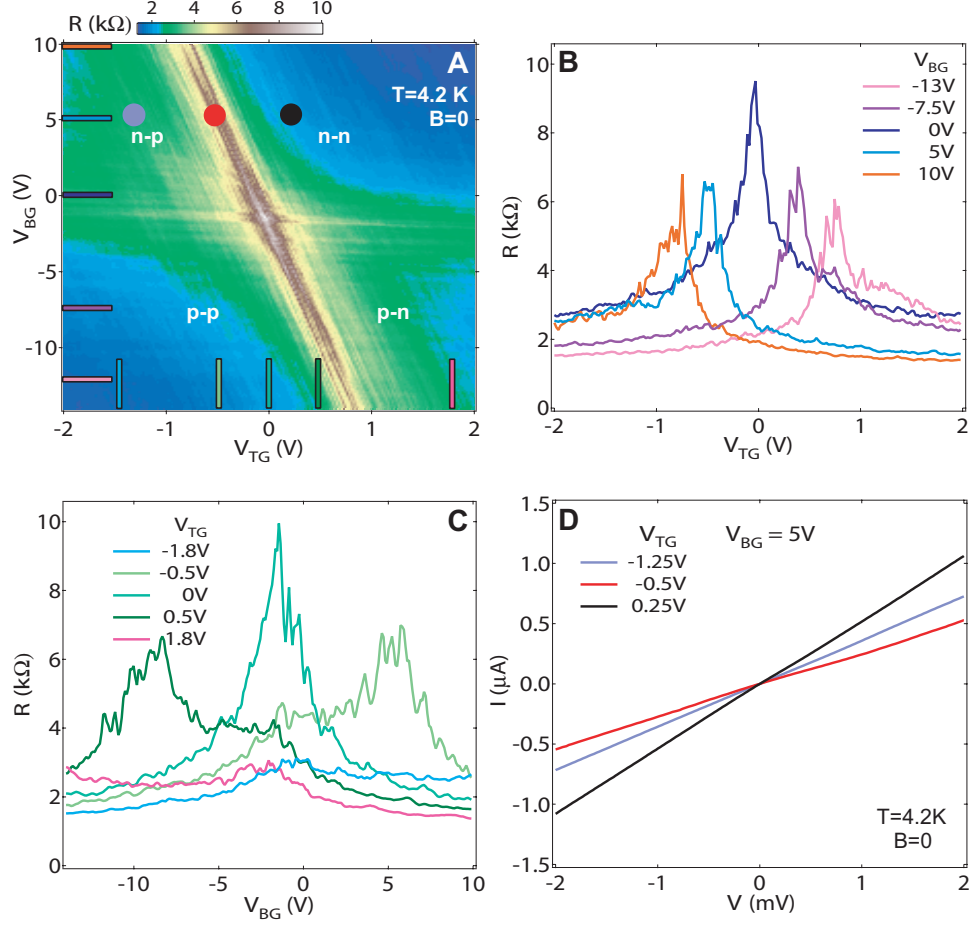


Figure 3.2: (a) Two-terminal differential resistance  $R$  as a function of the top-gate voltage  $V_{tg}$  and back-gate voltage  $V_{bg}$  at  $B_{\perp} = 0$  and  $T = 4.2$  K, demonstrating independent control of carrier type and density in regions 1 and 2. Labels in each of the four quadrants indicate the carrier type (first letter indicates carrier type in region 1). (b and c) Horizontal (Vertical) slices at  $V_{bg}$  ( $V_{tg}$ ) settings corresponding to the colored lines superimposed on Fig. 3.2(a). (d)  $I$ - $V$  curves at the gate voltage settings corresponding to the solid circles in Fig. 3.2(a) are representative of the linear characteristics observed everywhere in the plane of gate voltages.

asymmetry is studied in greater detail. The changing background resistance results from the different density in region 1 at each  $V_{bg}$  setting. Current-voltage ( $I$ - $V$ ) characteristics, measured throughout the  $(V_{tg}, V_{bg})$  plane, show no sign of rectification in any of the four quadrants or at either of the charge-neutral boundaries between quadrants [Fig. 3.2(d)], as expected for reflectionless (“Klein”) tunneling at the  $p$ - $n$  interface [16, 17].

### 3.5 Transport in the quantum Hall regime

At large  $B_{\perp}$ , the Dirac-like energy spectrum of graphene gives rise to a characteristic series of QH plateaus in conductance, reflecting the presence of a zero-energy Landau level, that includes only odd multiples of  $2 e^2/h$  (that is,  $2, 6, 10, \dots \times e^2/h$ ) for uniform carrier density in the sheet [11, 51, 52]. These plateaus can be understood in terms of an odd number of QH edge states (including a zero-energy edge state) at the edge of the sheet, circulating in a direction determined by the direction of  $B_{\perp}$  and the carrier type. The situation is somewhat more complicated when varying local density and carrier type across the sample.

A 2D color plot of differential conductance  $g = 1/R$  as a function of  $V_{bg}$  and  $V_{tg}$  at  $B_{\perp} = 4$  T is shown in Fig. 3.3(a). A vertical slice at  $V_{tg} = 0$  through the  $p$ - $p$  and  $n$ - $n$  quadrants [Fig. 3.3(b)] reveals conductance plateaus at  $2, 6$ , and  $10 e^2/h$  in both quadrants, demonstrating that the sample is single-layer and that the oxide does not significantly distort the Dirac spectrum.

QH features are investigated for differing filling factors  $\nu_1$  and  $\nu_2$  in regions 1 and 2 of the graphene sheet. A horizontal slice through Fig. 3.3(a) at filling factor  $\nu_1 = 6$  is shown in Fig. 3.3(c). Starting from the  $n$ - $n$  quadrant, plateaus are observed at  $6 e^2/h$  and  $2 e^2/h$  at top-gate voltages corresponding to filling factors  $\nu_2 = 6$  and  $2$ , respectively. Crossing over to the  $n$ - $p$  quadrant by further decreasing  $V_{tg}$ , a new plateau at  $3/2 e^2/h$  appears for  $\nu_2 = -2$ . In the  $\nu_2 = -6$  region, no clear QH plateau is observed. Another horizontal slice at  $\nu_1 = 2$  shows  $2 e^2/h$  plateaus at both  $\nu_2 = 6$  and  $2$  [see Fig. 3.3(d)]. Crossing into the  $n$ - $p$  quadrant, the conductance exhibits QH plateaus at  $1 e^2/h$  for  $\nu_2 = -2$  and near  $3/2 e^2/h$  for  $\nu_2 = -6$ .

For  $\nu_1$  and  $\nu_2$  of the same sign ( $n$ - $n$  or  $p$ - $p$ ), the observed conductance plateaus follow

$$g = \min(|\nu_1|, |\nu_2|) \times e^2/h. \quad (3.1)$$

This relation suggests that the edge states common to both regions propagate from source

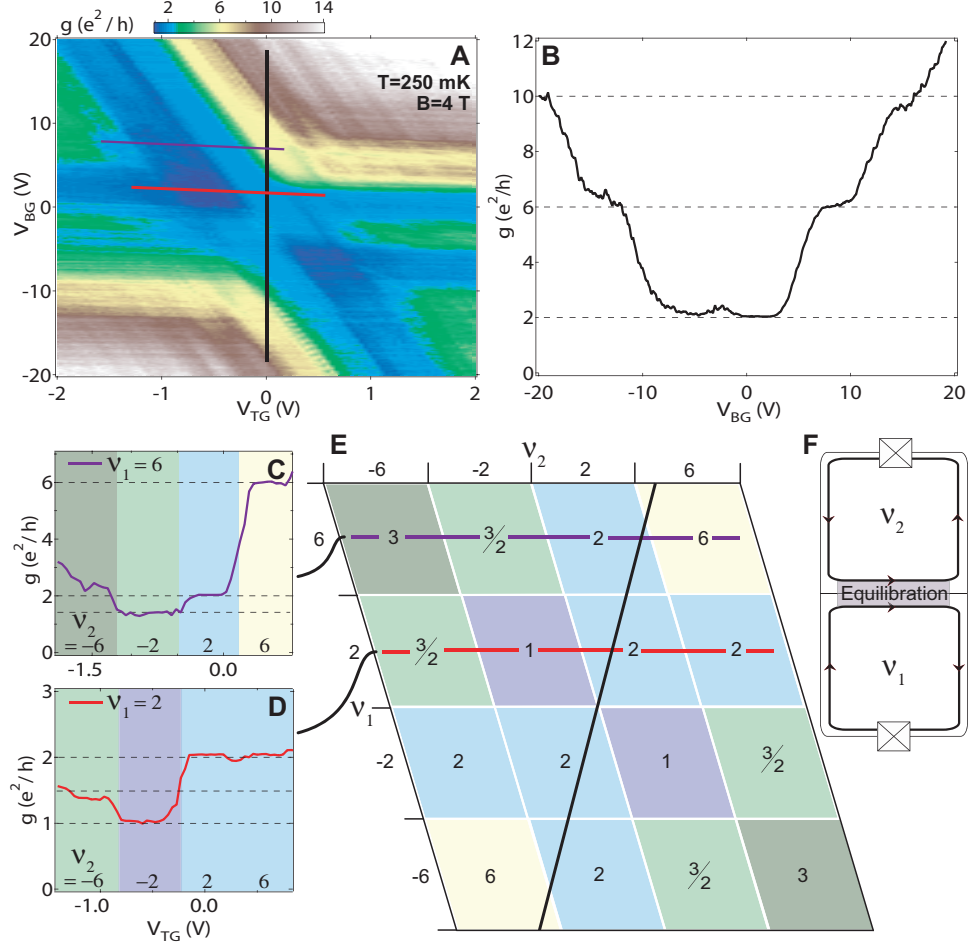


Figure 3.3: (a) Differential conductance  $g$  as a function of  $V_{tg}$  and  $V_{bg}$  at  $B_{\perp} = 4$  T and  $T = 250$  mK. (b) Vertical slice at  $V_{tg} = 0$ , traversing  $p$ - $p$  and  $n$ - $n$  quadrants. Plateaus are observed at  $2 e^2/h$  and  $6 e^2/h$ , the quantum Hall signature of single-layer graphene. (c) Horizontal slice at  $\nu_1 = 6$  showing conductance plateaus at  $6$ ,  $2$  and  $3/2 e^2/h$ . (d) Horizontal slice at  $\nu_2$  showing QH plateaus at  $2$ ,  $1$  and  $3/2 e^2/h$ . (e) Table of conductance plateau values as a function of filling factors calculated using Eqs. (3.1) and (3.2). Black, purple and red lines correspond to slices in (b), (c) and (d), respectively. (f) Schematic of counter-circulating edge states at filling factors  $\nu_1 = -\nu_2 = 2$ .

to drain while the remaining  $|\nu_1 - \nu_2|$  edge states in the region of highest absolute filling factor circulate internally within that region and do not contribute to the conductance. This picture is consistent with known results on conventional 2D electron gas systems with inhomogeneous electron density [53, 54, 55].

Recent theory [50] addresses QH transport for filling factors with opposite sign in regions

1 and 2 ( $n$ - $p$  and  $p$ - $n$ ). In this case, counter-circulating edge states in the two regions travel in the same direction along the  $p$ - $n$  interface [Fig. 3.3(f)], which presumably facilitates mode mixing between parallel-traveling edge states. For the case of complete mode-mixing—that is, when current entering the junction region becomes uniformly distributed among the  $|\nu_1| + |\nu_2|$  parallel-traveling modes—quantized plateaus are expected [50] at values

$$g = \frac{|\nu_1||\nu_2|}{|\nu_1| + |\nu_2|} \times e^2/h. \quad (3.2)$$

A table of the conductance plateau values given by Eqs. (3.1) and (3.2) is shown in Fig. 3.3(e). Plateau values at  $1 e^2/h$  for  $\nu_1 = -\nu_2 = 2$  and at  $3/2 e^2/h$  for  $\nu_1 = 6$  and  $\nu_2 = -2$  are observed in experiment. Notably, the  $3/2 e^2/h$  plateau suggests uniform mixing among four edge states (three from region 1 and one from region 2). All observed conductance plateaus are also seen at  $T = 4$  K and for  $B_\perp$  in the range 4 to 8 T.

We do find some departures between the experimental data and Eqs. (3.1) and (3.2), as represented in the grid of Fig. 3.3(e). For instance, the plateau near  $3/2 e^2/h$  in Fig. 3.3(d) is seen at a value of  $\sim 1.4 e^2/h$  and no clear plateau at  $3 e^2/h$  is observed for  $\nu_1 = -\nu_2 = 6$ . We speculate that the conductance in these regions being lower than their expected values is an indication of incomplete mode mixing. We also observe an unexpected peak in conductance at a region in gate voltage between the two  $1 e^2/h$  plateaus at  $\nu_1 = \pm\nu_2 = 2$ . This rise in conductance is clearly seen for  $|V_{\text{tg}}|$  values between  $\sim 1$  and 2 V and  $V_{\text{bg}}$  values between  $\sim -5$  and -2 V. This may result from the possible existence of puddles of electrons and holes near the charge-neutrality points of regions 1 and 2, as previously suggested [56].

## 3.6 Supplementary Information

### Graphene Preparation

Graphene is synthesized using a method similar to that pioneered in Ref. [5]. A thin piece of graphite is first extracted from a 5 mm square of highly oriented pyrolytic graphite

[SPI-1 grade from SPI supplies ([www.2spi.com](http://www.2spi.com))] using adhesive tape [3M Mask Plus II—Water Soluble Wave Solder Tape (<http://www.3m.com>)]. The graphite is thinned further by repeated exfoliation with tape. Prior to the final exfoliation, a  $n^{++}$  Si substrate with 300 nm thermally grown  $\text{SiO}_2$  is cleaned in acetone and isopropyl alcohol (IPA). Tape from the final exfoliation is immediately pressed against the substrate and rubbed gently with the back of a tweezer for  $\sim 10$  s. Following immersion in water at 60 °C to dissolve the tape, the substrate is again cleaned in acetone and IPA to remove any tape residue left on the substrate surface. The sample is next viewed under an optical microscope to identify potential single layers. Metallic contacts are then patterned as described in the main text.

## Oxide Layer Synthesis

The oxide separating the graphene sheet and metallic contact from the top gate consists of two layers: a non-covalent functionalization layer (NCFL) and  $\sim 30$  nm of Aluminum oxide ( $\text{Al}_2\text{O}_3$ ). Both layers are deposited using a Cambridge Nanotech Savannah Atomic Layer Deposition Tool (<http://www.cambridgenanotech.com>). The growth recipe described below is adapted from Ref. [39].

Immediately following a cleaning with acetone and IPA, the substrate is inserted into the atomic layer deposition (ALD) reaction chamber. The chamber is pumped down to a pressure of 0.3 torr. Next, NCFL is deposited at room temperature using 50 cycles of the following process. A 100 torr dose of  $\text{NO}_2$  gas is first introduced into the chamber for 0.5 s and then pumped out. Following a 7 s purge under continuous flow of 20 sccm of nitrogen gas ( $\text{N}_2$ ), a 1 torr dose of trimethylaluminum (TMA) vapor is pulsed into the chamber. The chamber is then purged for 2 min before beginning the next cycle. Ellipsometry measurements on trial runs show that the NCFL thickness remains constant for up to 125 cycles, indicating that NCFL growth is self-limiting, with only a single or few layers deposited on the graphene. The  $\text{Al}_2\text{O}_3$  is then grown by 305 ALD cycles, consisting of a 1 torr pulse of  $\text{H}_2\text{O}$  vapor and a 1.5 torr pulse of TMA vapor, under continuous flow

of  $N_2$  and with 5 s intervals between pulses. The first 5 cycles are performed at room temperature to prevent desorption of the NCFL. The remaining cycles are continued after heating the chamber to 225°C. With each  $H_2O$ -TMA cycle adding  $\sim 1$  Å of  $Al_2O_3$ , the total oxide thickness is  $\sim 30$  nm.

## Supporting Text

Measurements of differential conductance  $g$  as a function of top-gate voltage  $V_{tg}$  and back-gate voltage  $V_{bg}$  similar to those shown in Fig. 3.3A were performed at other temperatures  $T$  and magnetic fields  $B$ . A 2D image at  $T = 4.2$  K and  $B = 4$  T (Fig. 3.4A) reveals quantum Hall (QH) signatures similar to those observed at  $T = 250$  mK (Fig. 3.3A). The black curve in Fig. 3.4B is a slice at constant filling factor  $\nu_1 = 2$ . The same slice at  $T = 250$  mK, reproduced from Fig. 3.3D, is shown in red. The similarity between the two curves suggests that mode-mixing at the  $p$ - $n$  interface is only weakly dependent on temperature, most likely as a result of the large Landau level separation in graphene [11]. Data in Fig. 3.4A shows oscillations at high conductance ( $g \gtrsim 6 e^2/h$ ) in the  $p$ - $p$  and  $n$ - $n$  quadrants. We interpret these as Shubnikov-de Haas oscillations contributing to the two-terminal measurement.

2D images in Figures 3.4C and 3.4D show  $g$  at  $B = 8$  T for  $T = 4.2$  K and  $T = 250$  mK, respectively. A clear doubling of the Landau level spacing in gate voltage is observed in comparison to images at  $B = 4$  T (Figs. 3A and S1A). These data show cleaner conductance quantization in  $n$ - $n$  regions than in  $p$ - $p$  regions and also weak temperature dependence, as observed in Fig. 3.3A and 3.4A.

## 3.7 Acknowledgements

We thank L. S. Levitov, D. A. Abanin, C. H. Lewenkopf, and P. Jarillo-Herrero for useful discussions. We thank Z. Chen at IBM T. J. Watson Research Center for suggesting the

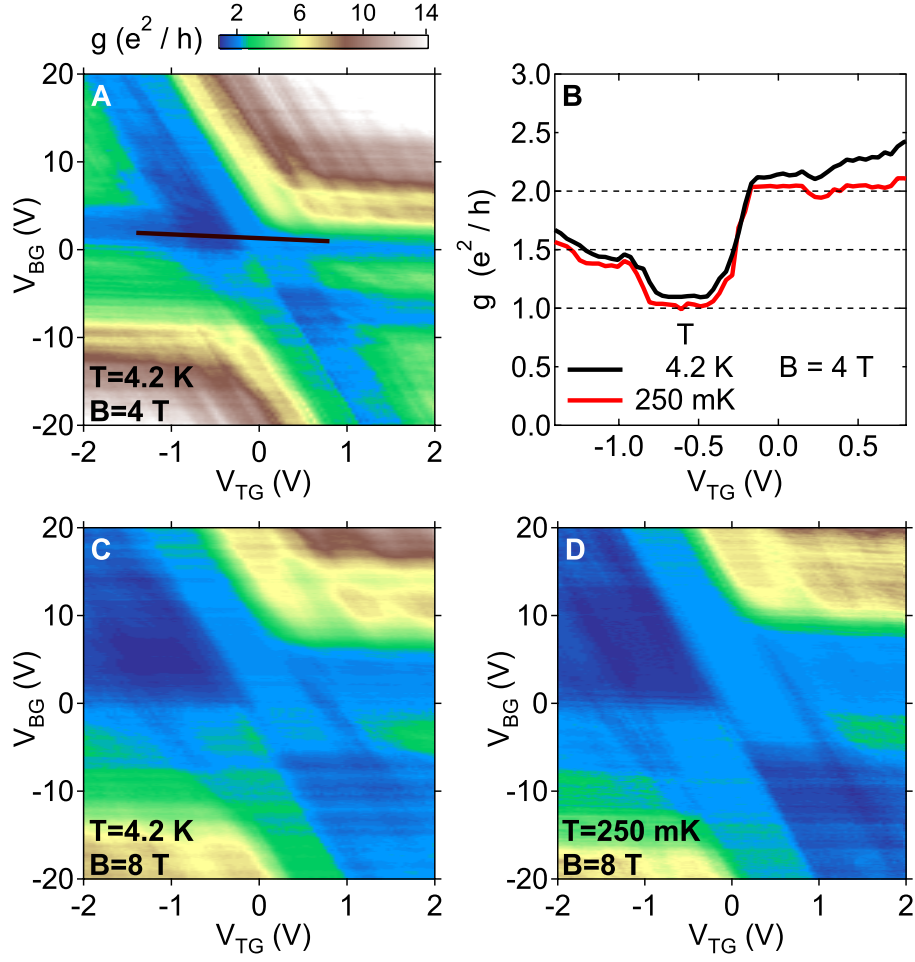


Figure 3.4: **A)** Differential conductance  $g$  as a function of top-gate voltage  $V_{tg}$  and back-gate voltage  $V_{bg}$  at  $T = 4.2$  K and  $B = 4$  T. **(B)** Slice of Fig. 3.4A at constant  $\nu_1 = 2$  (black). The same slice at  $T = 250$  mK is reproduced from Fig. 3.3D (red). **(C and D)**  $g$  as a function of  $V_{tg}$  and  $V_{bg}$  at  $B = 8$  T for temperatures of 4.2 K and 250 mK, respectively.

NO<sub>2</sub> functionalization process and D. Monsma for assistance in implementing it. Research supported in part by INDEX, an NRI Center, and by the Harvard NSEC.

## Chapter 4

# Shot noise in graphene

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We report measurements of current noise in single- and multi-layer graphene devices. In four single-layer devices, including a  $p$ - $n$  junction, the Fano factor remains constant to within  $\pm 10\%$  upon varying carrier type and density, and averages between 0.35 and 0.38. The Fano factor in a multi-layer device is found to decrease from a maximal value of 0.33 at the charge-neutrality point to 0.25 at high carrier density. These results are compared to theories for shot noise in ballistic and disordered graphene.<sup>1</sup>

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## 4.1 Introduction

Shot noise, the temporal fluctuation of electric current out of equilibrium, originates from the partial transmission of quantized charge [57]. Mechanisms that can lead to shot noise in mesoscopic conductors include tunneling, quantum interference, and scattering from impurities and lattice defects. Shot noise yields information about transmission that is not available from the dc current alone.

In graphene [7, 12], a zero-gap two-dimensional semi-metal in which carrier type and density can be controlled by gate voltages [5], density-dependent shot-noise signatures under various conditions have been investigated theoretically [16, 25]. For wide samples of ballistic graphene (width-to-length ratio  $W/L \gtrsim 4$ ) the Fano factor,  $\mathcal{F}$ , i.e., the current noise normalized to the noise of Poissonian transmission statistics, is predicted to be  $1/3$  at the charge-neutrality point and  $\sim 0.12$  in both electron ( $n$ ) and hole ( $p$ ) regimes [25]. The value  $\mathcal{F} = 1 - 1/\sqrt{2} \approx 0.29$  is predicted for shot noise across a ballistic  $p$ - $n$  junction [16]. For strong, smooth “charge-puddle” disorder, theory predicts  $\mathcal{F} \approx 0.30$  both at and away from the charge-neutrality point, for all  $W/L \gtrsim 1$  [58]. Disorder may thus have a similar effect on noise in graphene as in diffusive metals, where  $\mathcal{F}$  is universally  $1/3$  [59, 60, 61, 62, 63, 64] regardless of shape and carrier density. Recent theory investigates numerically the evolution from a density-dependent to a density-independent  $\mathcal{F}$  with increasing disorder [65]. To our knowledge, experimental data for shot noise in graphene has not yet been reported.

This chapter presents an experimental study of shot noise in graphene at low temperatures and zero magnetic field. Data for five devices, including a locally gated  $p$ - $n$  junction, are presented. For three globally-gated, single-layer samples, we find  $\mathcal{F} \sim 0.35 - 0.37$  in both electron and hole doping regions, with essentially no dependence on electronic sheet density,  $n_s$ , in the range  $|n_s| \lesssim 10^{12} \text{ cm}^{-2}$ . Similar values are obtained for a locally-gated single-layer  $p$ - $n$  junction in both unipolar ( $n$ - $n$  or  $p$ - $p$ ) and bipolar ( $p$ - $n$  or  $n$ - $p$ ) regimes. In a multi-layer sample, the observed  $\mathcal{F}$  evolves from  $0.33$  at the charge-neutrality point to

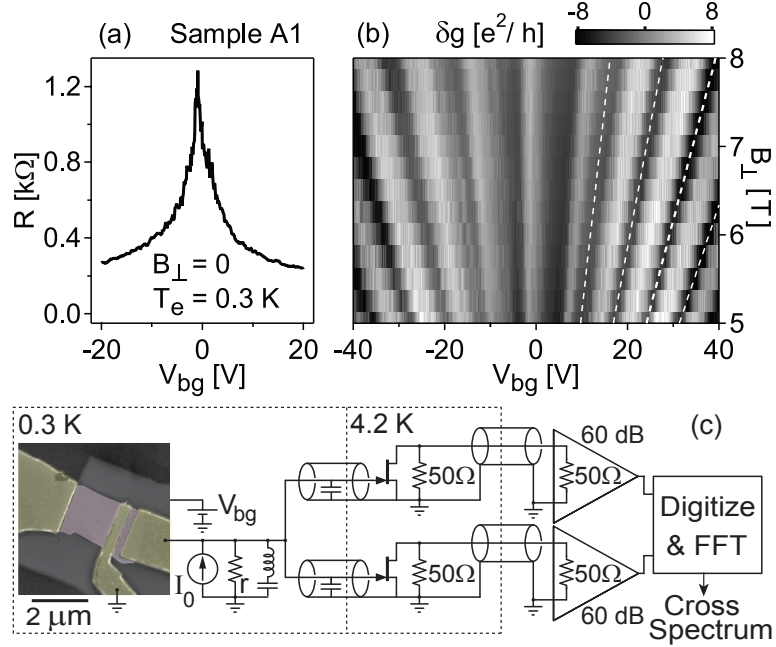


Figure 4.1: (a) Differential resistance  $R$  of sample A1 as a function of back-gate voltage  $V_{bg}$  at electron temperature  $T_e = 0.3$  K, perpendicular field  $B_{\perp} = 0$ , and source-drain voltage  $V_{sd} = 0$ . (b) Differential two-terminal conductance  $g(V_{sd} = 0)$  as a function of  $B_{\perp}$  and  $V_{bg}$  in the quantum Hall regime, after subtracting a quadratic fit at each  $B_{\perp}$ . Lines of constant filling factors 6, 10, 14, and 18 (dashed lines) indicate a single-layer sample. (c) Equivalent circuit near 1.5 MHz of the system measuring current noise using cross correlation of two channels [66]. Current bias  $I_o$  contains a 7.5 nA<sub>rms</sub>, 20 Hz part for lock-in measurements and a controllable dc part generating the dc component of  $V_{sd}$  via the shunt resistance  $r = 5$  k $\Omega$ . False-color scanning electron micrograph of a three-lead pattern defining two devices similar to A1 and A2. Purple indicates single-layer graphene and gold indicates metallic contacts.

0.25 at  $n_s \sim 6 \times 10^{12} \text{ cm}^{-2}$ .

## 4.2 Methods

Devices were fabricated by mechanical exfoliation of highly-oriented pyrolytic graphite [5]. Exfoliated sheets were deposited on a degenerately-doped Si substrate capped with 300 nm of thermally grown SiO<sub>2</sub>. Regions identified by optical microscopy as potential single-layer graphene were contacted with thermally evaporated Ti/Au leads (5/40 nm) patterned by electron-beam lithography. Additional steps in the fabrication of the  $p$ - $n$  junction device are detailed in Ref. [40]. Devices were measured in two <sup>3</sup>He cryostats, one allowing dc (lock-

in) transport measurements in fields  $|B_\perp| \leq 8$  T perpendicular to the graphene plane, and another allowing simultaneous measurements of dc transport and noise [66] near 1.5 MHz, but limited to  $B_\perp \sim 0$ .

### 4.3 Shot noise in single-layer devices

Differential resistance  $R = dV_{\text{sd}}/dI$  ( $I$  is the current, and  $V_{\text{sd}}$  is the source-drain voltage) of a wide, short sample [A1,  $(W, L) = (2.0, 0.35)$   $\mu\text{m}$ ] is shown as a function of back-gate voltage  $V_{\text{bg}}$  at  $V_{\text{sd}} = 0$  and  $B_\perp = 0$  in Fig. 4.1(a). While the width of the peak is consistent with A1 being single-layer graphene [9, 10], more direct evidence is obtained from the QH signature shown in Fig. 4.1(b). The grayscale image shows differential conductance  $g = 1/R$  as a function of  $V_{\text{bg}}$  and  $B_\perp$ , following subtraction of the best-fit quadratic polynomial to  $g(V_{\text{bg}})$  at each  $B_\perp$  setting to maximize contrast. Dashed lines correspond to filling factors  $n_s h/eB_\perp = 6, 10, 14$ , and  $18$ , with  $n_s = \alpha(V_{\text{bg}} + 1.1 \text{ V})$  and lever arm  $\alpha = 6.7 \times 10^{10} \text{ cm}^{-2}/\text{V}$ . Their alignment with local minima in  $\delta g(V_{\text{bg}})$  identifies A1 as single-layer graphene [33, 67]. The Drude mean free path  $\ell = h/2e^2 \cdot \sigma/k_F$  [68], where  $k_F = \sqrt{\pi|n_s|}$ , is found to be  $\sim 40$  nm away from the charge-neutrality point using the  $B_\perp = 0$  conductivity  $\sigma = (RW/L)^{-1}$  [Fig. 4.2(a) inset].

Current noise spectral density  $S_I$  is measured using a cross-correlation technique described in Ref. [66] [see Fig. 4.1(c)]. Following calibration of amplifier gains and electron temperature  $T_e$  using Johnson noise thermometry (JNT) for each cooldown, the excess noise  $S_I^e \equiv S_I - 4k_B T_e g(V_{\text{sd}})$  is extracted.  $S_I^e(V_{\text{sd}})$  for sample A1 is shown in Fig. 4.2(a). Linearity of  $S_I^e$  at high bias indicates negligible extrinsic ( $1/f$  or telegraph) resistance fluctuations within the measurement bandwidth. For these data, a single-parameter fit to the scattering-theory form (for energy-independent transmission) [69, 70],

$$S_I^e = 2eI\mathcal{F} \left[ \coth \left( \frac{eV_{\text{sd}}}{2k_B T_e} \right) - \frac{2k_B T_e}{eV_{\text{sd}}} \right], \quad (4.1)$$

gives a best-fit Fano factor  $\mathcal{F} = 0.349$ . Simultaneously measured conductance  $g \approx 22.2 e^2/h$

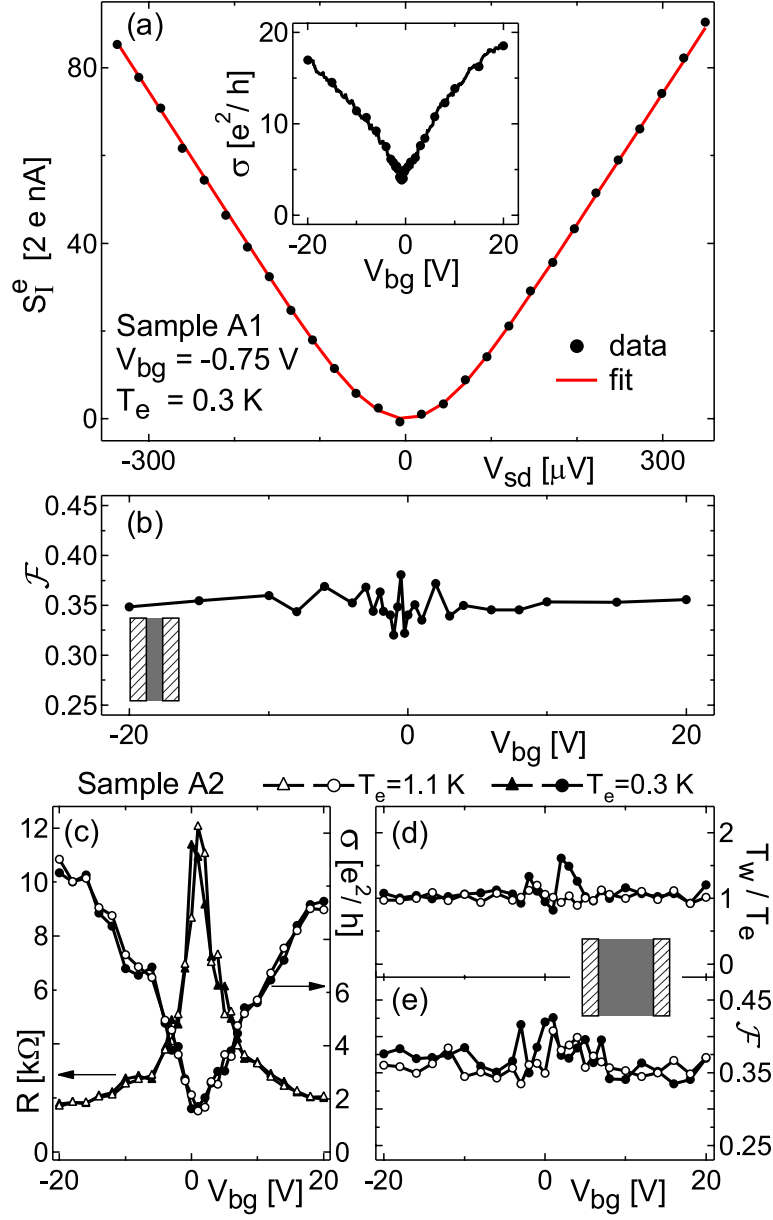


Figure 4.2: (a) Inset: Conductivity  $\sigma = (RW/L)^{-1}$  calculated using  $R(V_{bg})$  data in Fig. 4.1(a) and  $W/L = 5.7$ . Solid black circles correspond to  $\sigma(V_{sd} = 0)$  at the  $V_{bg}$  settings of noise measurements shown in (b). Main: Excess noise  $S_I^e$  as function of  $V_{sd}$  near the charge-neutrality point,  $V_{bg} = -0.75$  V. The solid red curve is the single-parameter best fit to Eq. (4.1), giving Fano factor  $\mathcal{F} = 0.349$  (using  $T_e = 303$  mK as calibrated by JNT). (b) Best-fit  $\mathcal{F}$  at 25  $V_{bg}$  settings across the charge-neutrality point for electron and hole densities reaching  $|n_s| \sim 1.4 \times 10^{12} \text{ cm}^{-2}$ . (c)  $R$  (left axis) and  $\sigma$  (right axis) of sample A2 as a function of  $V_{bg}$  ( $W/L = 1.4$ ), with  $V_{sd} = 0$ , at 0.3 K (solid markers) and at 1.1 K (open markers). (d), (e) Crossover width  $T_w$  (normalized to JNT-calibrated  $T_e$ ) and  $\mathcal{F}$ , obtained from best-fits using Eq. (4.1) to  $S_I^e(V_{sd})$  data over  $|V_{sd}| \leq 350(650) \mu\text{V}$  for  $T_e = 0.3(1.1)$  K.

was independent of bias within  $\pm 0.5\%$  (not shown) in the  $|V_{\text{sd}}| \leq 350 \mu\text{V}$  range used for the fit. Note that the observed quadratic-to-linear crossover agrees well with that in the curve fit, indicating weak inelastic scattering in A1 [62, 63], and negligible series resistance (e. g., from contacts), which would broaden the crossover by reducing the effective  $V_{\text{sd}}$  across the sample.

Figure 4.2(b) shows similarly measured values for  $\mathcal{F}$  as a function of  $V_{\text{bg}}$ .  $\mathcal{F}$  is observed to remain nearly constant for  $|n_{\text{s}}| \lesssim 10^{12} \text{ cm}^{-2}$ . Over this density range, the average  $\mathcal{F}$  is 0.35 with standard deviation 0.01. The estimated error in the best-fit  $\mathcal{F}$  at each  $V_{\text{bg}}$  setting is  $\pm 0.002$ , comparable to the marker size and smaller than the variation in  $\mathcal{F}$  near  $V_{\text{bg}} = 0$ , which we believe results from mesoscopic fluctuations of  $\mathcal{F}$ . Nearly identical noise results (not shown) were found for a similar sample (B), with dimensions  $(2.0, 0.3) \mu\text{m}$  and a QH signature consistent with a single layer.

Transport and noise data for a more square single-layer sample [A2, patterned on the same graphene sheet as A1, with dimensions  $(1.8, 1.3) \mu\text{m}$ ] at  $T_e = 0.3 \text{ K}$  (solid circles) and  $T_e = 1.1 \text{ K}$  (open circles) are shown in Figs. 4.2(c-e). At both temperatures, the conductivity shows  $\sigma_{\text{min}} \approx 1.5 e^2/h$  and gives  $\ell \sim 25 \text{ nm}$  away from the charge-neutrality point. That these two values differ from those in sample A1 is particularly notable as samples A1 and A2 were patterned on the same piece of graphene. Results of fitting Eq. (4.1) to  $S_I^e(V_{\text{sd}})$  for sample A2 are shown in Figs. 4.2(d) and 4.2(e). To allow for possible broadening of the quadratic-to-linear crossover by series resistance and/or inelastic scattering, we treat electron temperature as a second fit parameter (along with  $\mathcal{F}$ ) and compare the best-fit value,  $T_{\text{w}}$ , with the  $T_e$  obtained from Johnson noise. Figure 4.2(d) shows  $T_{\text{w}}$  tracking the calibrated  $T_e$  at both temperatures. Small deviations of  $T_{\text{w}}/T_e$  from unity near the charge-neutrality point at  $T_e = 0.3 \text{ K}$  can be attributed to conductance variations up to  $\pm 20\%$  in the fit range  $|V_{\text{sd}}| \leq 350 \mu\text{V}$  at these values of  $V_{\text{bg}}$ . As in sample A1,  $\mathcal{F}$  is found to be independent of carrier type and density over  $|n_{\text{s}}| \lesssim 10^{12} \text{ cm}^{-2}$ , averaging  $0.37(0.36)$  with standard deviation  $0.02(0.02)$  at  $T_e = 0.3(1.1) \text{ K}$ . Evidently, despite its different aspect

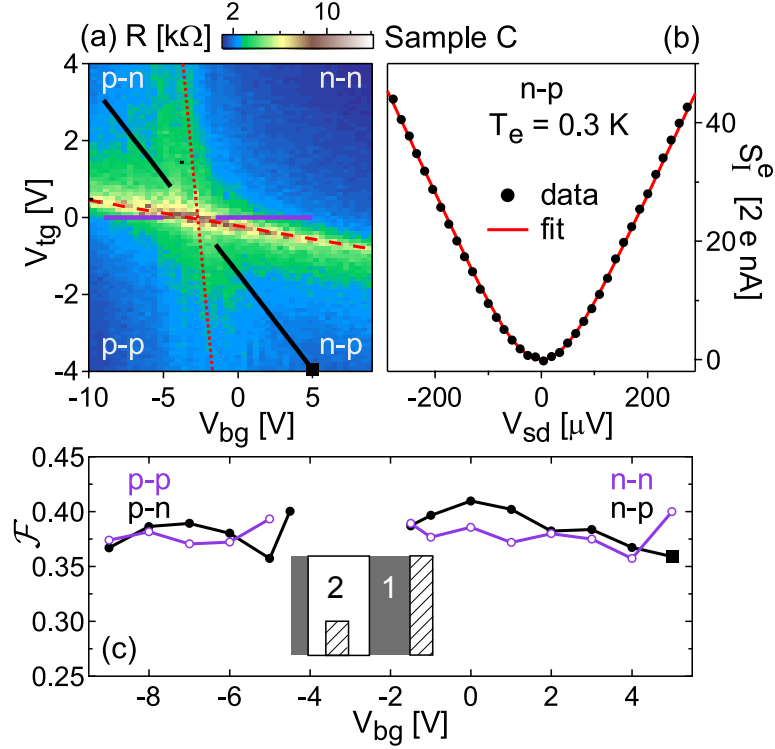


Figure 4.3: (a) Differential resistance  $R$  of sample C, a single-layer  $p$ - $n$  junction, as a function of back-gate voltage  $V_{bg}$  and top-gate voltage  $V_{tg}$ . The skewed-cross pattern defines quadrants of  $n$  and  $p$  carriers in regions 1 and 2. Red lines indicate charge-neutrality lines in region 1 (dotted) and region 2 (dashed). (b)  $S_I^e(V_{sd})$  measured in  $n$ - $p$  regime with  $(V_{bg}, V_{tg}) = (5, -4)$  V (solid dots) and best fit to Eq. (4.1) (red curve), with  $\mathcal{F} = 0.36$ . (c) Main: Best-fit  $\mathcal{F}$  along the cuts shown in (a), at which  $n_{s1} \sim n_{s2}$  (purple) and  $n_{s1} \sim -4 n_{s2}$  (black). Inset: Schematic of the device. The top gate covers region 2 and one of the contacts.

ratio, A2 exhibits a noise signature similar to that of A1.

#### 4.4 Shot noise in a $p$ - $n$ junction

Transport and noise measurements for a single-layer graphene  $p$ - $n$  junction [40], sample C, are shown in Fig. 4.3. The color image in Fig. 4.3(a) shows differential resistance  $R$  as a function of  $V_{bg}$  and local top-gate voltage  $V_{tg}$ . The two gates allow independent control of charge densities in adjacent regions of the device [see Fig. 4.3(c) inset]. In the bipolar regime, the best-fit  $\mathcal{F}$  shows little density dependence and averages 0.38, equal to the average value deep in the unipolar regime, and similar to results for the back-gate-only single-layer

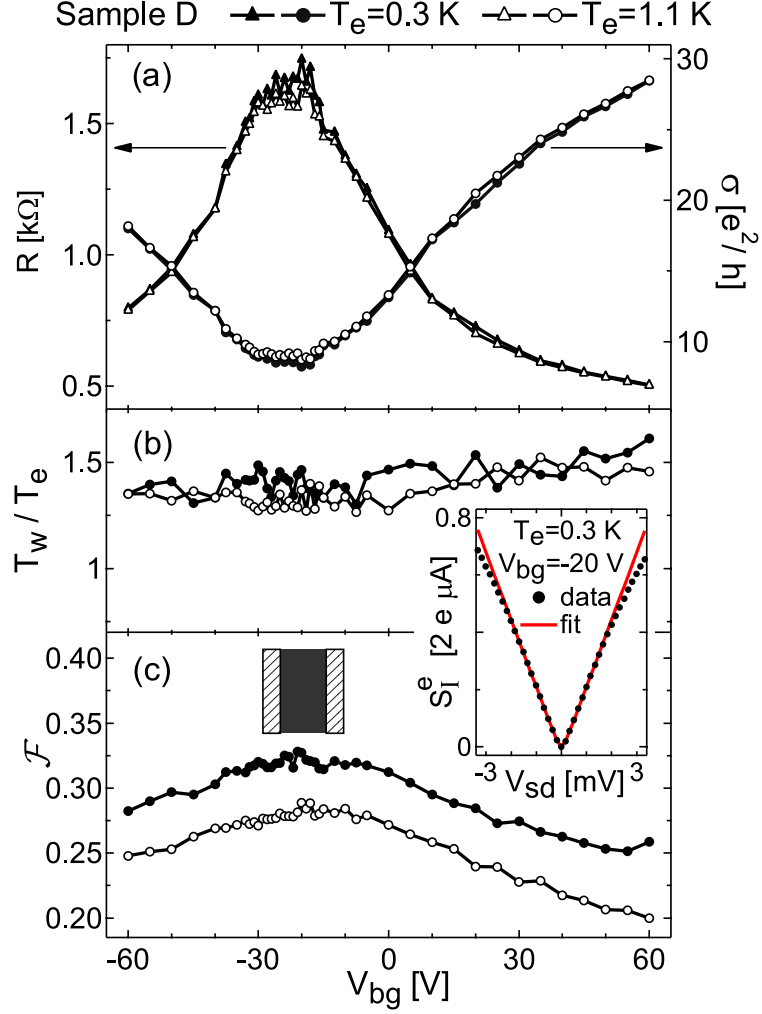


Figure 4.4: (a) Differential resistance  $R$  (left axis) and conductivity  $\sigma$  (right axis) of sample D as a function of  $V_{bg}$ , with  $V_{sd} = 0$ , at 0.3 K (solid markers) and at 1.1 K (open markers). (b),(c) Best-fit  $T_w$  (normalized to JNT-calibrated  $T_e$ ) and  $\mathcal{F}$  to  $S_I^e(V_{sd})$  data over  $|V_{sd}| \leq 0.5(1)$  mV for  $T_e = 0.3(1.1)$  K. Inset: Sublinear dependence of  $S_I^e$  on  $V_{sd}$  is evident in data taken over a larger bias range. Solid red curve is the two-parameter best fit of Eq. (4.1) over  $|V_{sd}| \leq 0.5$  mV.

samples (A1, A2 and B). Close to charge neutrality in either region (though particularly in the region under the top gate),  $S_I^e(V_{sd})$  deviates from the form of Eq. (4.1) (data not shown). This is presumably due to resistance fluctuation near charge neutrality, probably due mostly to mobile traps in the  $Al_2O_3$  insulator beneath the top gate.

## 4.5 Shot noise in a multi-layer device

Measurements at 0.3 K and at 1.1 K for sample D, of dimensions (1.8, 1.0)  $\mu\text{m}$ , are shown in Fig. 4.4. A  $\sim 3$  nm step height between  $\text{SiO}_2$  and carbon surfaces measured by atomic force microscopy prior to electron-beam lithography [71] suggests this device is likely multi-layer. Further indications include the broad  $R(V_{\text{bg}})$  peak [72] and the large minimum conductivity,  $\sigma_{\text{min}} \sim 8 e^2/h$  at  $B_{\perp} = 0$  [Fig. 4.4(a)], as well as the absence of QH signature for  $|B_{\perp}| \leq 8$  T at 250 mK (not shown). Two-parameter fits of  $S_I^e(V_{\text{sd}})$  data to Eq. (4.1) show three notable differences from results in the single-layer samples [Figs. 4.4(b) and 4.4(c)]: First,  $\mathcal{F}$  shows a measurable dependence on back-gate voltage, decreasing from 0.33 at the charge-neutrality point to 0.25 at  $n_s \sim 6 \times 10^{12} \text{ cm}^{-2}$  for  $T_e = 0.3$  K; Second,  $\mathcal{F}$  decreases with increasing temperature; Finally,  $T_w/T_e$  is 1.3-1.6 instead of very close to 1. We interpret the last two differences, as well as the sublinear dependence of  $S_I^e$  on  $V_{\text{sd}}$  (see Fig. 4.4 inset) as indicating sizable inelastic scattering [59, 60] in sample D. (An alternative explanation in terms of series resistance would require it to be density, bias, and temperature dependent, which is inconsistent with the independence of  $g$  on  $V_{\text{sd}}$  and  $T_e$ ).

## 4.6 Summary and acknowledgements

Summarizing the experimental results, we find that in four single-layer samples,  $\mathcal{F}$  is insensitive to carrier type and density, temperature, aspect ratio, and the presence of a  $p$ - $n$  junction. In one multi-layer sample,  $\mathcal{F}$  does depend on density and temperature, and  $S_I^e(V_{\text{sd}})$  shows a broadened quadratic-to-linear crossover and is sublinear in  $V_{\text{sd}}$  at high bias. We may now compare these results to expectations based on theoretical and numerical results for ballistic and disordered graphene.

Theory for ballistic single-layer graphene with  $W/L \gtrsim 4$  gives a universal  $\mathcal{F} = 1/3$  at the charge-neutrality point, where transmission is evanescent, and  $\mathcal{F} \sim 0.12$  for  $|n_s| \gtrsim \pi/L^2$ , where propagating modes dominate transmission [25]. While the measured  $\mathcal{F}$  at the charge-

neutrality point in samples A1 and B ( $W/L = 5.7$  and  $6.7$ , respectively) is consistent with this prediction, the absence of density dependence is not:  $\pi/L^2 \sim 3 \times 10^9 \text{ cm}^{-2}$  is well within the range of carrier densities covered in the measurements. Theory for ballistic graphene  $p$ - $n$  junctions [16] predicts  $\mathcal{F} \approx 0.29$ , lower than the value  $\sim 0.38$  observed in sample C in both  $p$ - $n$  and  $n$ - $p$  regimes. We speculate that these discrepancies likely arise from the presence of disorder. Numerical results for strong, smooth disorder [58] predict a constant  $\mathcal{F}$  at and away from the charge-neutrality point for  $W/L \gtrsim 1$ , consistent with experiment. However, the predicted value  $\mathcal{F} \approx 0.30$  is  $\sim 20\%$  lower than observed in all single-layer devices. Recent numerical simulations [65] of small samples ( $L = W \sim 10 \text{ nm}$ ) investigate the vanishing of carrier dependence in  $\mathcal{F}$  with increasing disorder strength. In the regime where disorder makes  $\mathcal{F}$  density-independent, the value  $\mathcal{F} \sim 0.35 - 0.40$  is found to depend weakly on disorder strength and sample size.

Since theory for an arbitrary number of layers is not available for comparison to noise results in the multi-layer sample D, we compare only to existing theory for ballistic bi-layer graphene [73]. It predicts  $\mathcal{F} = 1/3$  over a much narrower density range than for the single layer, and abrupt features in  $\mathcal{F}$  at finite density due to transmission resonances. A noise theory beyond the bi-layer ballistic regime may thus be necessary to explain the observed smooth decrease of  $\mathcal{F}$  with increasing density in sample D.

We thank C. H. Lewenkopf, L. S. Levitov, and D. A. Abanin for useful discussions. Research supported in part by the IBM Ph.D. Fellowship program (L.D.C.), INDEX, an NRI Center, and Harvard NSEC.

## Chapter 5

# Quantum Hall conductance of two-terminal graphene devices

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Measurement and theory of the two-terminal conductance of monolayer and bilayer graphene in the quantum Hall regime are compared. We examine features of conductance as a function of gate voltage that allow monolayer, bilayer, and gapped samples to be distinguished. In particular, we analyze the distortions of quantum Hall plateaus and the conductance peaks and dips at the charge neutrality point, which can be used to identify the incompressible densities. These results are compared to recent theory and possible origins of the discrepancy are discussed.<sup>1</sup>

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<sup>1</sup>This chapter was submitted to Physical Review B

## 5.1 Introduction

Graphene monolayers and bilayers are recently discovered two-dimensional gapless semimetals. The Dirac spectrum of excitations in monolayer graphene gives rise to a number of novel transport properties, including anomalous quantized Hall conductance with plateaus at  $4(n+1/2)e^2/h$ ,  $n = 0, \pm 1, \pm 2, \dots$  in multiterminal samples [9, 10]. Bilayer graphene has a quadratic, electron-hole-symmetric excitation spectrum, leading to quantized Hall conductance values  $4ne^2/h$ ,  $n = \pm 1, \pm 2, \dots$  [7, 13]. Both monolayer and bilayer graphene have a zeroth Landau level, located at the charge neutrality point (CNP), which is eightfold degenerate in bilayers and fourfold degenerate in monolayers. Other Landau levels are all fourfold degenerate in both types of graphene [11, 52, 67]. The novel transport signatures not only reflect this underlying band structure, but serve as an experimental tool for identifying the number of layers and characterizing sample quality [7].

In recent work on graphene, two-terminal magnetoconductance has emerged as one of the main tools of sample characterization [40, 45, 74]. While a two-terminal measurement is not as straightforward to interpret as the corresponding multiterminal measurement [14], it is the simplest to perform and may be the only measurement possible, for instance with very small samples. The presence of non-zero longitudinal conductivity causes quantum Hall plateaus measured in a two-terminal configuration to not be as well quantized as in multiprobe measurement [7]. As discussed in detail below, plateaus exhibit a characteristic N-shaped distortion arising from the finite longitudinal conductivity that depends on device geometry.

In this Article, we systematically examine two-terminal conductance in the QH regime for monolayer and bilayer graphene for a variety of sample aspect ratios (Table 5.1). We especially focus on the features that can help to distinguish monolayer and bilayer graphene: the conductance extrema in the N-shaped distortions of the quantum Hall plateaus and at the CNP. We find that these features depend on the sample aspect ratio and on the number

of graphene layers.

Results are compared to recent theory [75], in which two-terminal conductance for arbitrary shape is characterized by a single parameter  $\xi$ , the effective device aspect ratio ( $\xi = L/W$  for rectangular samples, where  $L$  is the length or distance between contacts, and  $W$  is the device width). The N-shaped distortions of the plateaus, arranged symmetrically around the CNP, are consistently observed in the two-terminal conductance measured as a function of carrier density, both in the data presented in this paper and elsewhere [40, 74, 45]. The overall behavior of the conductance is in good qualitative agreement with theoretical results [75].

Table 5.1: Measured two-terminal graphene devices.

Sample	Layers (Inferred)	$(L, W)$ [ $\mu\text{m}$ ]	$\xi_s$	$\xi_{\text{fit}}$
A1	Monolayer	(1.3, 1.8)	0.7	1.7
A2	Monolayer	(0.4, 2.0)	0.2	0.2
B1	Bilayer	(2.5, 1.0)	2.5	0.8
B2	Bilayer	(0.3, 1.8)	0.2	0.3
C	Monolayer	Asymmetric	0.9 <sup>1</sup>	0.9

In Ref. [75], the positions of conductance extrema on the distorted plateaus were found to align with the incompressible densities, where the centers of quantized plateaus occur in multiterminal devices. In particular, it was predicted that in short samples ( $\xi < 1$ ) the conductance minima are centered around the incompressible densities. On the other hand, for narrow samples ( $\xi > 1$ ) the maxima of the conductance are expected to occur at the incompressible densities. Here we demonstrate that this relation can be used to distinguish monolayer and bilayer graphene devices even when the distortions of the plateaus are strong. We find that the maxima (or the minima) line up with incompressible densities precisely in the way expected for the monolayer and bilayer graphene.

The correlation between the maxima (minima) and incompressible densities is unambiguous; it is supported by all measurements presented in the paper. We analyze data for several rectangular two-terminal samples as well as for one sample with asymmetric contacts, extracting an effective sample aspect ratio via conformal mapping. Best-fit values of the aspect ratio,  $\xi_{\text{fit}}$ , obtained by fitting the theory to the experimental data, are compared to the measured sample aspect ratio,  $\xi_s$ . Agreement between data and theory is relatively good for the samples of smaller lengths, and less good for the longer ( $L \gtrsim 1 \mu\text{m}$ ) samples. We speculate on possible causes of these discrepancies, including inhomogeneous contact resistance, electron and hole puddles, and contributions of transport along  $p$ - $n$  interfaces.

## 5.2 Phenomenology of conductance in two-terminal graphene devices

Representative theoretical plots of two-terminal conductance for monolayer, bilayer, and gapped bilayer graphene as a function of filling factor,  $\nu$ , are shown in Fig. 5.1. For both monolayers and bilayers, the absence of an energy gap between the conduction and valence bands gives rise to a zero energy Landau level (LL)[11], which can either increase or decrease the two-terminal conductance around the charge neutrality point, depending on the aspect ratio of the sample. The eightfold degeneracy of the zero-energy LL in bilayer graphene [67] enhances the size of this feature relative to monolayer graphene.

A gap in the spectrum of bilayer graphene opens when the on-site energy in one layer differs from the on-site energy in the other [67]. This may result, for instance, from asymmetric chemical doping [76] or electrostatic gating [77]. The gap splits the zero-energy LL, suppressing conductance at the CNP. The qualitative effect of a gap in the bilayer spectrum can be seen in Fig. 5.1 by comparing the gapped case [Fig. 5.1(c)], which always has a zero of conductance at  $\nu = 0$ , to the gapless cases [Figs. 1(a,b)], which has a non-zero value of conductance at  $\nu = 0$ .

Also illustrated in Fig. 5.1 is how the aspect ratio of the sample affects the two-terminal conductance near quantum Hall plateaus for all three spectrum types. Finite longitudinal conductivity leads to N-shaped distortions of the plateaus [75], which are of opposite signs for aspect ratios  $\xi < 1$  and  $\xi > 1$ . Note, however, that the extrema of conductance—minima for  $\xi < 1$  and maxima for  $\xi > 1$ —are aligned with the plateaus centers, which coincide with the incompressible density values (different for monolayers and bilayers). Distorted plateaus thus remain useful for characterizing the number of layers and density.

The back-gate dependence of conductance for the five samples reported are most similar to those in Figs. 1(a,b), indicating that these samples are single layers and gapless bilayers only (see Table 1). We use the model of Ref. [75] to fit the conductance data treating the aspect ratio as a fit parameter. In doing so, our presumption is that the visible dimensions of the sample may not reflect the actual pattern of current flow. Since the conductance problem for a sample of any shape can be reduced to that of an effective rectangle via a conformal mapping [78, 79, 80], which depends on the sample shape but not on the conductivity tensor, the rectangular geometry is universal for two-terminal conductance. Thus the model of a conducting rectangle with an unspecified aspect ratio is suitable for describing systems in which current pattern is not precisely known.

### 5.3 Sample fabrication and measurement

Graphene devices were fabricated by mechanically exfoliating highly oriented pyrolytic graphite [5] onto a  $n^{++}$  Si wafer capped with  $\sim 300$  nm of  $\text{SiO}_2$ . Potential single and bilayer graphene flakes were identified by optical microscopy. Source and drain contacts, defined by electron beam lithography, were deposited by thermally evaporating 5/40 nm of Ti/Au. The aspect ratio,  $\xi_s$ , of each sample was measured using either optical or scanning electron microscopy after transport measurements were performed.

Devices were measured in a  $^3\text{He}$  refrigerator allowing dc transport measurements in a

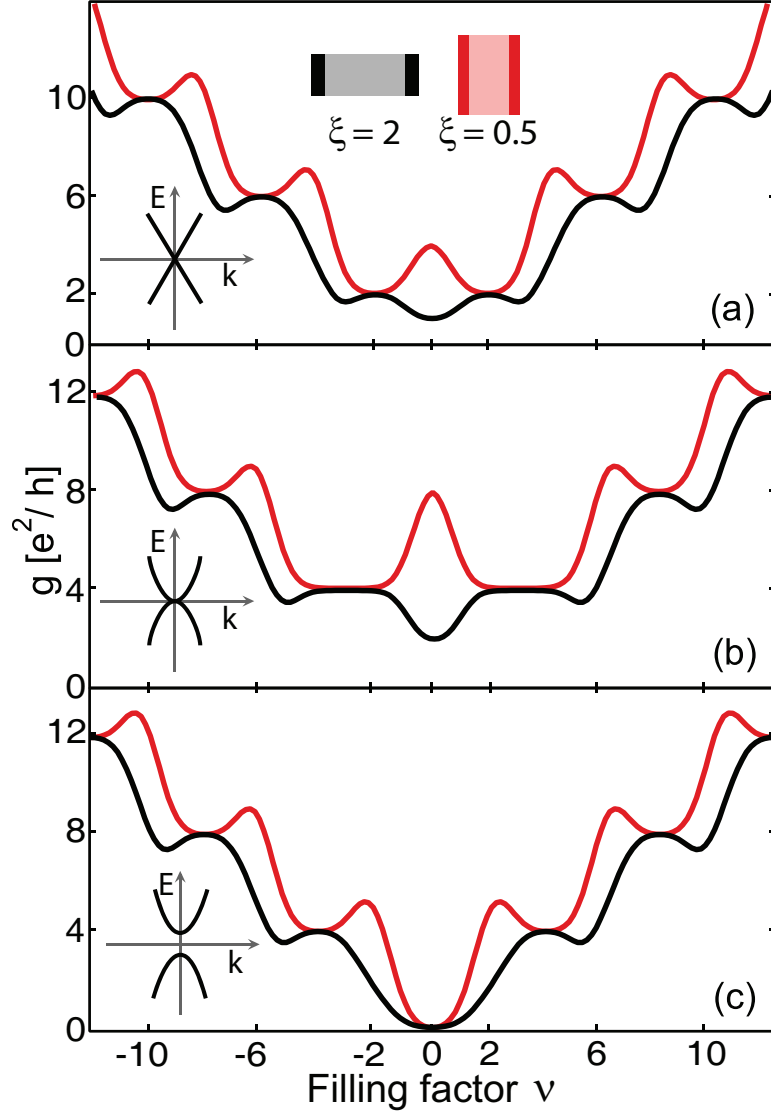


Figure 5.1: Theoretical [75] two-terminal QH conductance  $g$  as a function of filling factor  $\nu$  for (a) single-layer graphene, (b) bilayer graphene, and (c) gapped bilayer graphene, for effective aspect ratios  $\xi = L/W = 2$  (black) and  $0.5$  (red). Finite longitudinal conductivity due to the states in the middle of each Landau level distorts the plateaus into N-shaped structures, which are of opposite sign for  $\xi < 1$  and  $\xi > 1$ . Local extrema of  $g$  at filling factors  $\nu = \pm 2, \pm 6, \pm 10 \dots$  for single layers and at  $\nu = \pm 4, \pm 8, \pm 12 \dots$  for bilayers are either all maxima ( $\xi > 1$ ) or all minima ( $\xi < 1$ ). For gapless monolayer and bilayer samples (a,b),  $g(\nu = 0)$  is a maximum for  $\xi < 1$  and minimum for  $\xi > 1$ ; for the gapped bilayer (c)  $g$  vanishes at  $\nu = 0$  for all  $\xi$ .

magnetic field  $|B| < 8$  T perpendicular to the graphene plane. Unless otherwise noted, all measurements were taken at base temperature,  $T \sim 250$  mK. Differential conductance  $g = dI/dV$ , where  $I$  is the current and  $V$  the source-drain voltage, was measured using a

current bias ( $I$  chosen to keep  $eV < k_B T$ ) and standard lock-in technique at a frequency of 93 Hz. All samples show  $B = 0$  characteristics of high-quality single-layer and bilayer graphene [9, 10]: a CNP positioned at back-gate voltage  $V_{\text{bg}} \sim 0$  V and a change in  $g$  exceeding  $20 e^2/h$  over the  $V_{\text{bg}}$  range of  $\pm 40$  V.

## 5.4 Monolayer samples

Figure 2(a) shows the two-terminal conductance  $g(V_{\text{bg}})$  for sample A1 ( $\xi_s = 0.7$ ) at  $B = 8$  T (black trace). Plateaus are seen at  $\nu = \pm 2$  near—but not equal to— $2 e^2/h$ , with values of  $\sim 2.3(2.7) e^2/h$  on the electron (hole) side of the CNP. At the CNP ( $V_{\text{bg}} \sim 2.3$  V, obtained from  $g$  at  $B = 0$ ),  $g$  departs from the quantized values, dropping to a minimum of  $\sim 1.4 e^2/h$ . At higher densities, the conductance exhibits a series of maxima with values slightly above 6, 10,  $14 e^2/h$ . Maxima on the hole side consistently have slightly higher values, a feature observed in all the samples measured. The inset of Fig. 5.2(a) shows  $g$  in the QH regime as a function of  $V_{\text{bg}}$  and  $B$ . Dashed black lines indicating the filling factors  $\nu = n_s h / eB$  (where  $n_s$  is the carrier density) of  $-6$ ,  $-10$ ,  $-14$ , and  $-18$  align with the local *maxima* of  $g(V_{\text{bg}}, B)$ . Here,  $V_{\text{bg}}$  was converted to  $n_s$  using a parallel plate capacitance model[5], giving  $n_s = \alpha(V_{\text{bg}} + V_{\text{offset}})$  with  $\alpha = 6.7 \times 10^{10} \text{ cm}^{-2} \text{ V}^{-1}$  and  $V_{\text{offset}} = 2$  V. Although the values of  $V_{\text{bg}}$  at the CNP and  $V_{\text{offset}}$  are slightly different, we note that the value of  $V_{\text{bg}}$  for the CNP is not well defined below  $\sim 2$  V - a result of the underlying disorder in the sample [33] - and since these two values do not differ by more than this value we do not ascribe any significance to this discrepancy.

Measured  $g(V_{\text{bg}})$  [black curve in Fig. 5.2(b)] for sample A2 ( $\xi_s = 0.2$ ), made using the same graphene flake as A1, shows distinctive differences from the measured  $g(V_{\text{bg}})$  of sample A1. In particular, at the CNP ( $V_{\text{bg}} = -1.5$  V),  $g$  exhibits a sharp peak with a maximal value  $\sim 8.8 e^2/h$ . Away from the CNP, the conductance has maxima which are much stronger than those of sample A1. The inset of Fig. 5.2(b) shows  $g(V_{\text{bg}}, B)$ . For this

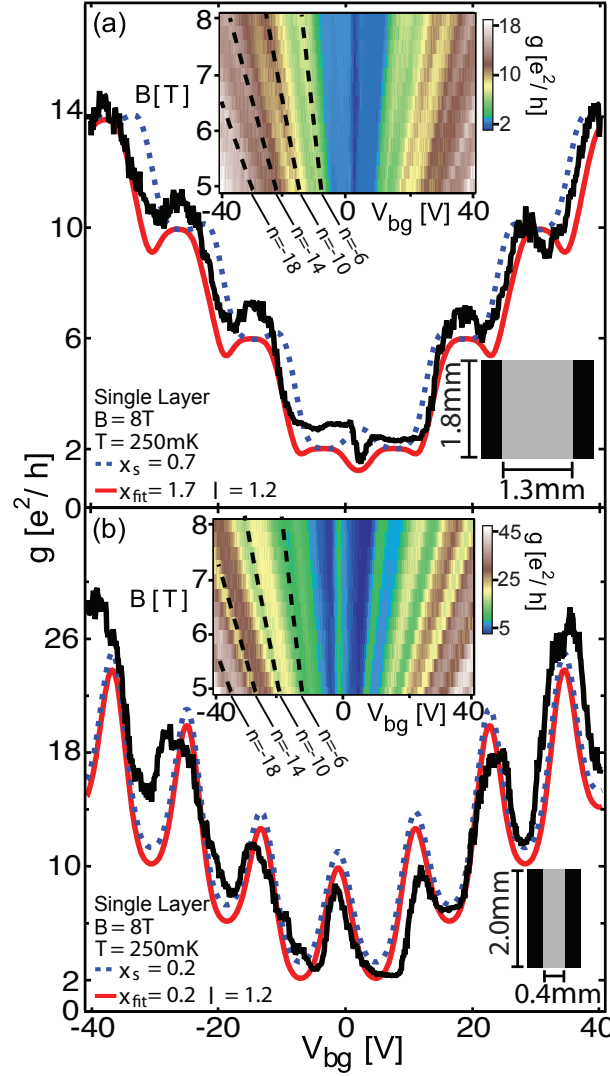


Figure 5.2: (a) Inset: Conductance  $g$  in the quantum Hall regime as a function of  $B$  and  $V_{bg}$  at  $T = 250\text{mK}$  for sample A1. Black dashed lines correspond to filling factors  $\nu = -6, -10, -14, -18$  and align with the local *maxima* of conductance. Main: (black) Horizontal cut of inset giving  $g(V_{bg})$  at  $B = 8\text{ T}$  and calculated  $g$  for the best-fit equivalent aspect ratio  $\xi_{fit} = 1.7$  (solid red curve) and for the measured sample aspect ratio  $\xi_s = 0.7$  (dashed blue curve) using Landau level broadening parameter  $\lambda = 1.2$ . (b) Inset: Conductance  $g$  in the quantum Hall regime as a function of  $B$  and  $V_{bg}$  at  $T = 250\text{mK}$  for sample A2. Black dashed lines correspond to  $\nu = -6, -10, -14, -18$  and align with the local *minima* of conductance. Main: (black) Horizontal cut of inset giving  $g(V_{bg})$  at  $B = 8\text{ T}$  and calculated  $g$  for  $\xi_{fit} = 0.2$  (solid red curve) and  $\xi_s = 0.2$  (dashed blue curve) ( $\lambda = 1.2$ , the same as sample A1). The dashed blue curve was vertically displaced for clarity.

sample, the dashed lines representing the incompressible filling factors  $-6, -10, -14, -18$  now align with the *minima* in  $g$ . Here we used  $\alpha = 6.7 \times 10^{10} \text{ cm}^{-2} \text{ V}^{-1}$  (the same as for sample A1) and  $V_{\text{offset}} = -1.1 \text{ V}$ .

The observed features in  $g$  for samples A1 and A2 can be compared to theory [75] for two-terminal quantum Hall conductance, which uses a model of a conducting rectangle  $L \times W$  with a spatially uniform conductivity. The filling factor dependence of the conductivity tensor is obtained using the semicircle relation for quantum Hall systems, derived in Ref. [81], which is applied independently for each Landau level. Landau level broadening due to disorder is included in the theory as a gaussian broadening  $e^{-\lambda(\nu-\nu_n)^2}$ , where  $\nu_n$  is the center of the LL and  $\lambda$  is a fitting parameter. The total conductivity tensor is taken to be a sum of the contributions of individual Landau levels. The current-density distribution for a rectangular sample with an arbitrary aspect ratio is found analytically by conformal mapping ([78, 79, 80]). The current density is then integrated numerically along suitably chosen contours to evaluate total current and voltage drop, from which  $g = I/V$  is obtained.

Along with the experimental traces, Figs. 2(a,b) also show the theoretical curves for  $\xi_{\text{fit}}$  (solid red trace) and for  $\xi_s$  (dashed blue trace) ratios. For sample A1  $\xi_{\text{fit}} = 1.7$ , differs considerably from  $\xi_s = 0.7$ . For sample A1, the best fit gives  $\lambda = 1.2$ . This theoretical curve ( $\xi_{\text{fit}} = 1.7$ ) reproduces the essential features of the data: local maxima align with the filling factors  $\pm 2, \pm 6, \pm 10, \dots$ , and  $g$  exhibits a dip at the CNP.

The alignment of conductance minima with densities corresponding to the integer filling factors as well as a peak at the CNP observed for sample A2 are consistent with theoretical predictions for a short, wide monolayer graphene sample. As illustrated in Fig. 5.2(b),  $\xi_{\text{fit}} = 0.2$  matches the measured  $\xi_s$  for sample A2.

We observe that the size of peaks and dips in Fig. 5.2(a,b) increases for higher LL. In contrast, theory [75] predicts that peaks and dips at  $|\nu| > 0$  LLs are all roughly the same. This discrepancy may reflect the inapplicability of the two-phase model approach of Ref. [81], which underlies the semicircle law obtained in this work, to higher LLs. Indeed,

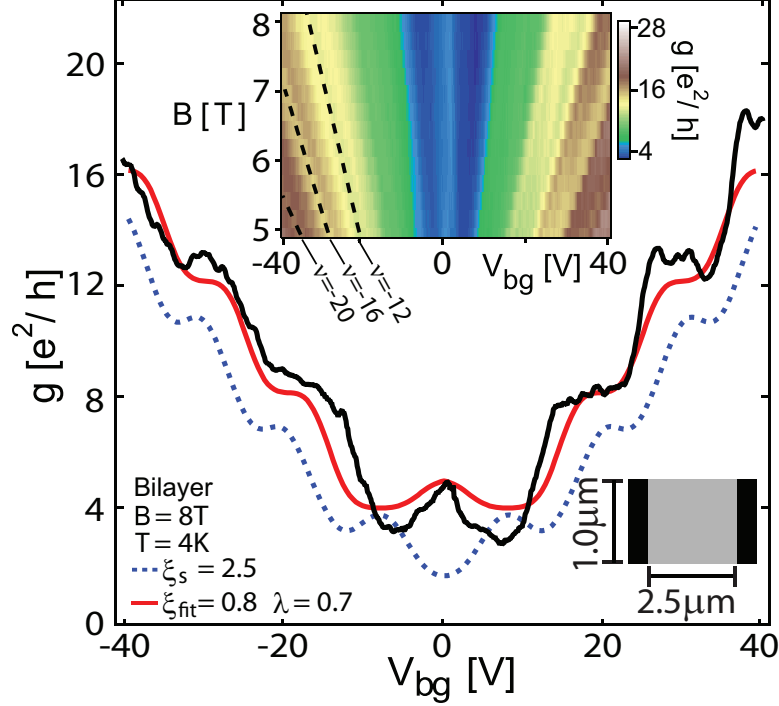


Figure 5.3: (a) Inset: Conductance  $g$  in the quantum Hall regime as a function of  $B$  and  $V_{bg}$  at  $T = 250$  mK for sample A1. Black dashed lines correspond to filling factors  $\nu = -6, -10, -14, -18$  and align with the local *maxima* of conductance. Main: (black) Horizontal cut of inset giving  $g(V_{bg})$  at  $B = 8$  T and calculated  $g$  for the best-fit equivalent aspect ratio  $\xi_{fit} = 1.7$  (solid red curve) and for the measured sample aspect ratio  $\xi_s = 0.7$  (dashed blue curve) using Landau level broadening parameter  $\lambda = 1.2$ . (b) Inset: Conductance  $g$  in the quantum Hall regime as a function of  $B$  and  $V_{bg}$  at  $T = 250$  mK for sample A2. Black dashed lines correspond to  $\nu = -6, -10, -14, -18$  and align with the local *minima* of conductance. Main: (black) Horizontal cut of inset giving  $g(V_{bg})$  at  $B = 8$  T and calculated  $g$  for  $\xi_{fit} = 0.2$  (solid red curve) and  $\xi_s = 0.2$  (dashed blue curve) ( $\lambda = 1.2$ , the same as sample A1). The dashed blue curve was vertically displaced for clarity.

because for Dirac particles the spacing between LLs decreases at higher energies as an inverse square root of the level number, one may expect mixing between non-nearest LLs to increase at high energies. Such mixing can lead to the longitudinal conductivity values in excess of those of Ref. [81], which only considers mixing between nearest LLs (see the discussion in Ref. [82]).

To take these effects into account, we extend the model of Ref. [75] by assuming that the contribution of the  $n^{\text{th}}$  LL to the conductivity tensor in monolayer graphene is described

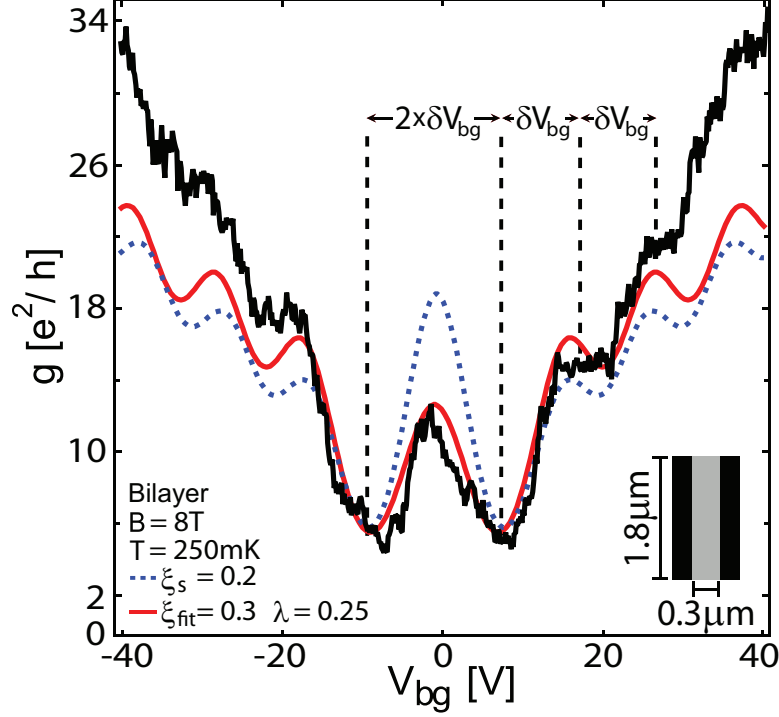


Figure 5.4: Measured  $g(V_{\text{bg}})$  for sample B2 (black) and the calculated  $g$  using  $\lambda = 0.25$  for  $\xi_s = 0.2$  (dashed blue trace) and  $\xi_{\text{fit}} = 0.3$  (solid red trace). Two key features in the curve suggest this sample is a gapless bilayer, namely, a pronounced peak in  $g$  near the CNP, and the larger spacing between the two minima straddling the CNP compared to the spacing  $\delta V_{\text{bg}} \sim 9.5$  V between other consecutive minima.

by a modified semicircle (“elliptic”) law,

$$\delta_n \sigma_{xx}^2 + A_n^2 (\delta_n \sigma_{xy} - \sigma_{xy,n}^0) (\delta_n \sigma_{xy} - \sigma_{xy,n'}^0) = 0, \quad (5.1)$$

where  $\delta_n \sigma_{xx}$  and  $\delta_n \sigma_{xy}$  are the effective longitudinal and Hall conductivities,  $\sigma_{xy,n}^0$  and  $\sigma_{xy,n'}^0$  are the quantized Hall conductivities at the neighboring plateaus. Here  $n$  and  $n'$  are neighboring LL indices, related by  $n' = n + 1$  (except the doubly degenerate  $\nu = 0$  LL for the bilayer, in which case  $n = -1$  and  $n' = 1$ ). The  $A_n$  account for departures from the semicircle law. We take  $A_n \approx 1$  for  $n = 0, \pm 1$ , and  $A_n \approx 2$  for other LLs, consistent with previous observations [82].

## 5.5 Bilayer samples

The black curve in Fig. 5.3 shows measured  $g(V_{\text{bg}})$  for sample B1 ( $\xi_s = 2.5$ ) at  $B = 8$  T and  $T = 4$  K. This sample has two features indicating that it is a bilayer sample: plateaus in conductance appearing near  $4$ ,  $8$ ,  $12$  and  $16 e^2/h$ , and a conductance maximum at the CNP whose relative size is much larger than those at higher LLs. The conductance values at the plateaus  $\nu = \pm 4$  here are lower than the expected  $4 e^2/h$  for a bilayer sample, falling to  $2.7(3.1) e^2/h$  on the electron (hole) side of the CNP. The peak value in conductance at  $\nu = 0$  ( $V_{\text{bg}} = 0.5$  V) is  $5 e^2/h$ . At higher filling factors, the plateaus exhibit two different behaviors, showing a flat plateau at  $\nu = 8$  and a plateau followed by a dip at  $\nu = 12$ . The small dips align with the filling factors  $\nu = -12, -16, -20$  for  $5 \text{ T} < B < 8 \text{ T}$  (see inset of Fig. 5.3), using  $\alpha = 7.2 \times 10^{10} \text{ cm}^{-2} \text{ V}^{-1}$  and  $V_{\text{offset}} = 0.5$  V.

Theoretical  $g$  curves for aspect ratios  $\xi_s = 2.5$  (dashed blue curve) and  $\xi_{\text{fit}} = 0.8$  (solid red curve) are shown in Fig. 5.3. Theoretical  $g(V_{\text{bg}})$  curves for these two aspect ratios are similar at high density, but differ for  $\nu = 0$ : the curve for  $\xi_s = 2.5$  has a dip in conductance at the CNP while  $\xi_{\text{fit}} = 0.8$  has a peak, similar to the experimental curve. The curve for  $\xi_{\text{fit}} = 0.8$  also agrees better with experiment at higher densities.

In some cases the two-terminal geometry can strongly distort the conductance, leading to a large difference between values of the two-terminal conductance at the local extrema and the quantized conductance values observed in multiterminal samples. In sample B2 (Fig. 5.4),  $g$  reaches a maximum of  $13.5 e^2/h$  at the CNP, with adjacent minima of  $5 e^2/h$ . Away from the CNP, conductance plateaus appear at values of  $\sim 16 e^2/h$  and  $23 e^2/h$ , neither of which are near expected values for monolayer or bilayer graphene. Since there are no strong peaks or dips in  $g$  away from charge neutrality, as is expected for a device with a  $\xi_s \ll 1$ , it is difficult to determine the number of layers from the location of the conductance extrema. There are two conductance features, however, that suggest the sample is gapless bilayer graphene. First, the peak at  $\nu = 0$  is much more pronounced than any other peak

in the conductance. Second, the spacing in  $V_{\text{bg}}$  between the two lowest LLs is twice as large as the spacing between any other two successive LLs (in Fig. 5.4,  $\delta V_{\text{bg}} \sim 9.5 \text{ V}$ ). Both features arise in bilayers as a result of the zero-energy LL being eightfold degenerate, twice as much as all other bilayer LLs and the zero-energy LL in single layer graphene [67]. The theoretical result for  $\xi_{\text{fit}} = 0.3$  (solid red line) and  $\xi_s = 0.2$  (dashed blue line), for sample B2 are shown in Fig. 5.4.

## 5.6 Non-rectangular samples

In this section we extend the comparison of theory and experiment to a non-rectangular device, sample C, shown schematically in the inset of Fig. 5.5. The measured two-terminal conductance of sample C (black curve in Fig. 5.5) has properties very similar to those expected for a square monolayer sample: around the CNP the conductance is nearly flat with value  $\sim 2e^2/h$ , monotonically increasing on the electron and hole sides at filling factors  $|\nu| > 2$ .

Theoretical curve shown in Fig. 5 is obtained from the conducting rectangle model using  $\xi_{\text{fit}} = 0.9$  and  $\lambda = 0.7$ . This choice of parameters yields particularly good agreement for  $|\nu| \leq 6$ . At higher fillings, the plateaus are washed out, suggesting that the LL broadening is stronger for LLs  $|n| \geq 2$ . It is interesting to compare  $\xi_{\text{fit}}$  to an effective aspect ratio, obtained from conformal mapping of sample C to a rectangle. As discussed below, this conformal mapping can be constructed directly, owing to the relatively simple geometry of sample C. The effective aspect ratio obtained in this way is  $\xi_s \approx 0.9$ , consistent with  $\xi_{\text{fit}}$ .

Before we proceed to construct the conformal mapping we note that the geometry of sample C, pictured in Fig. 5.6, is that of a polygon. In principle, any polygon can be mapped onto the upper half-plane by inverting a Schwarz-Christoffel mapping [83]. However, since this mapping is defined by a contour integral, the inverse mapping can only be found numerically. In order to circumvent this difficulty, two approximations are employed below,

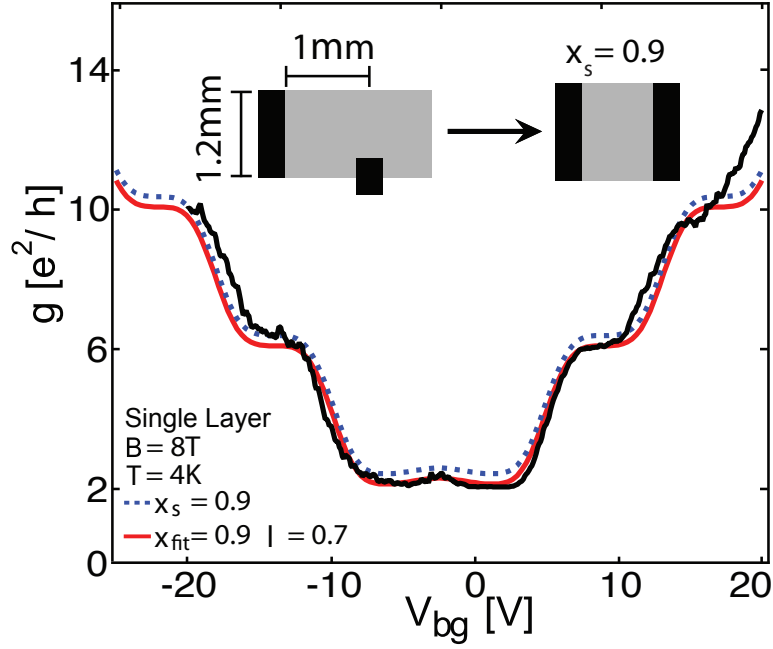


Figure 5.5: Measured  $g(V_{bg})$  for sample C (black) and calculated conductance (solid red curve) for  $\xi_{fit} = 0.9$  ( $\lambda = 0.7$ ). The asymmetric contacts of this sample can be conformally mapped onto a rectangle, producing a device aspect ratio of  $\xi_s = 0.9$  (dashed blue curve). The dashed blue curve was vertically displaced for clarity.

allowing the desired mapping to be constructed as a composition of a few simple mappings.

The steps involved in this construction are illustrated in Fig. 5.7. First, the rectangular shape in Fig. 6 is replaced by a semi-infinite strip shown in Fig. 5.7(a). This approximation should not significantly affect the conductance, as the current flows mostly in the region between contacts 1-2 and 3-4. Without loss of generality we set the length scale  $a = 1$ .

The next step is to straighten out the contact 3-5-6-4. For that, let us consider an auxiliary mapping that maps the upper  $\tilde{w}$  plane onto the upper  $\tilde{z}$  plane with a removed rectangle [84]:

$$\tilde{z} - iA = \int_0^{\tilde{w}} \left( \frac{\xi^2 - 1}{\xi^2 - 2} \right)^{1/2} d\xi. \quad (5.2)$$

We choose the parameter  $A$  to be equal

$$A = \int_0^1 \left( \frac{\xi^2 - 1}{\xi^2 - 2} \right)^{1/2} d\xi \approx 0.60, \quad (5.3)$$

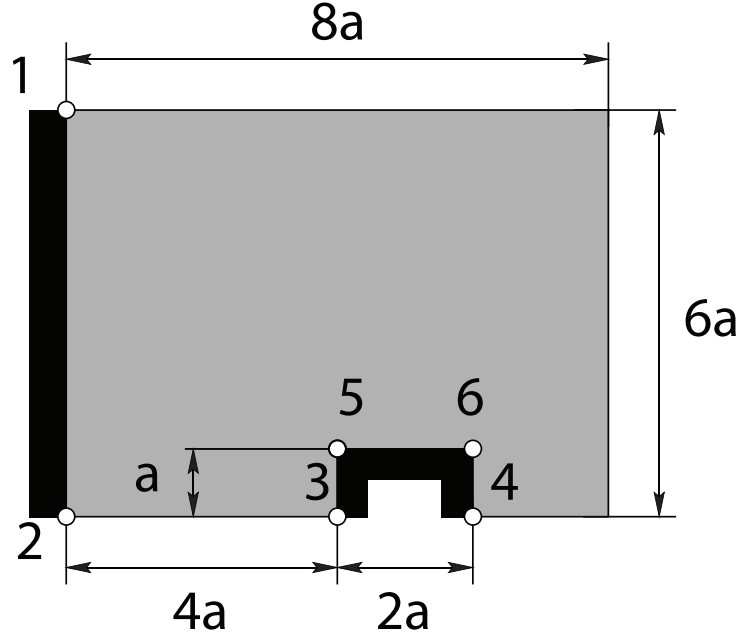


Figure 5.6: A polygon representing sample C (see Fig. 5.5). Black regions correspond to contacts (length scale  $a = 200$  nm).

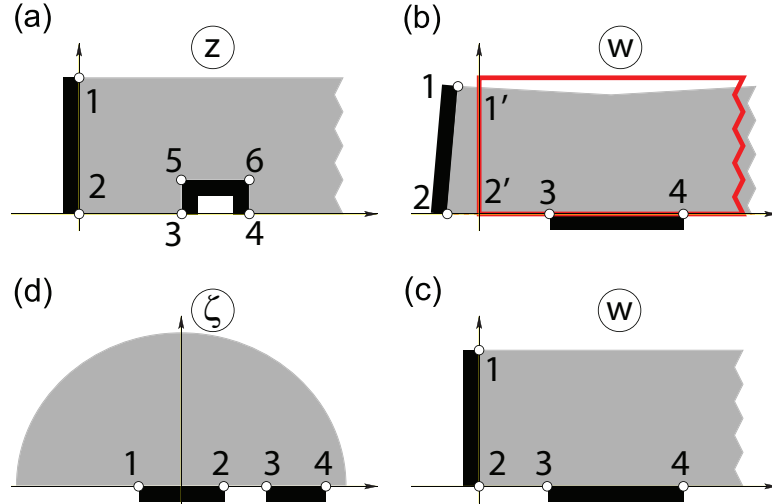


Figure 5.7: Three steps used to map the polygon in Fig. 5.6 (sample C) onto the upper half-plane (schematic). First, the rectangle in Fig. 5.6 is replaced by a half-infinite strip, extending indefinitely to the right (a). Next, we map the domain shown in (a) onto a rectangle with contact 3-5-6-4 straightened out (b). Under this mapping, the sample is slightly distorted, as indicated by the grey polygon in (b). Because the deviation of the grey polygon boundary from the original sample boundary [red line in (b)] is fairly small, it can be neglected, giving a half-infinite strip (c). Finally, the domain (c) is mapped onto the upper half-plane (d), which allows to find the cross ratio  $\Delta_{1234}$ , Eq. (5.9), and evaluate the effective aspect ratio, Eq. (5.10).

so that the removed rectangle has vertices

$$\tilde{z}_{3,4} = \pm A, \quad \tilde{z}_{5,6} = \pm A + iA. \quad (5.4)$$

These points correspond to the points  $\tilde{w}_{3,4} = \pm\sqrt{2}$ ,  $\tilde{w}_{5,6} = \pm 1$  in the  $\tilde{w}$  plane. The value of  $A$  ensures that the edge of the sample on the  $x$  axis remains on the  $x$  axis under the mapping (5.2). The distance between points  $\tilde{z}_3$  and  $\tilde{z}_5$  plane equals  $A$ , as follows from Eq. (5.2) and the identity

$$\int_1^{\sqrt{2}} \left| \frac{\xi^2 - 1}{\xi^2 - 2} \right|^{1/2} d\xi = \int_0^1 \left( \frac{\xi^2 - 1}{\xi^2 - 2} \right)^{1/2} d\xi, \quad (5.5)$$

which can be proved by making the change of variables,  $\xi = \sqrt{2 - x}$  in the integral in the left-hand side of Eq. (5.5), and  $\xi = \sqrt{x}$  in the integral in the right-hand side of Eq. (5.5).

The removed rectangle has aspect ratio equal to 2, the same as that for the contact 3-5-6-4, however, their dimensions differ by a factor of  $A$ . Scaling and shifting both  $\tilde{z}$  in  $\tilde{w}$ ,

$$\tilde{z} = A(z - 5), \quad \tilde{w} = A(w - 5), \quad (5.6)$$

we obtain the required mapping which straightens out the contact 3-5-6-4.

The second approximation is necessary because the mapping (5.2), (5.6), while straightening the segments 3-5-6-4, distorts the rest of the boundary. We notice, however, that sufficiently far from the contact 3-5-6-4 the mapping (5.2) is close to the identity:

$$z(w \gg 1) = w + O(1/w), \quad |z - 5| \gg 1. \quad (5.7)$$

This property and the relatively small size of the segments 3-5-6-4 compared to the strip width guarantees that the distortion is small. This is shown schematically in Fig. 5.7(b), where the curved grey polygon represents the actual image of the sample, with the deviation of its boundary from the strip of the same asymptotic width (shown in red and exaggerated for clarity). The deviation is indeed small: by investigating the mapping (5.2), (5.6) numerically we found that the boundary is displaced the most at point 2 which is shifted

by approximately 0.3 away from its original position  $2'$  along the real axis. This is small compared to the sample width, equal to 6, which allows us to neglect the displacement of the boundary. Thus we assume that the mapping (5.2), (5.6) transforms sample C into the semi-infinite strip shown in Fig. 5.7(c).

After this approximation is made, it is straightforward to transform the semi-infinite strip in Fig. 5.7(c) into the upper half-plane, which can be done by the mapping

$$\zeta = \cosh \frac{\pi w}{6}. \quad (5.8)$$

In the  $\zeta$  plane, the contacts are mapped on the real axis, with the end points 1, 2, 3 and 4 mapped to  $\zeta_1 = -1$ ,  $\zeta_2 = 1$ ,  $\zeta_3 \approx 2.11$ ,  $\zeta_4 \approx 23.57$ . From these values, following the procedure described in Ref. [[75]] (Appendix), we compute the cross ratio

$$\Delta_{1234} = \frac{(\zeta_1 - \zeta_4)(\zeta_3 - \zeta_2)}{(\zeta_1 - \zeta_2)(\zeta_3 - \zeta_4)} \approx -0.64, \quad (5.9)$$

and then obtain the aspect ratio from the relations

$$\xi_s = \frac{L}{W} = \frac{K(k')}{2K(k)}; \quad \Delta_{1234} = (1 - k^2)/2k, \quad (5.10)$$

where  $K(k)$  is the complete elliptic integral of the first kind, and  $k' = (1 - k^2)^{1/2}$ . This procedure yields the value  $\xi_s = 0.9$ , identical to that found from the best fit to a conducting rectangle model (see Fig. 5).

## 5.7 Summary and discussion

In summary, we have studied the effect of geometry on the conductance of two-terminal graphene devices in the QH regime, comparing experiment and theory. The QH plateaus typically exhibit conductance extrema that are stronger for wide, short samples. For wide samples ( $\xi_{\text{fit}} < 1$ ), minima of the two-terminal conductance are expected at filling factors where plateaus would be found in multiterminal devices. On the other hand, for narrow samples ( $\xi_{\text{fit}} > 1$ ), conductance maxima appear at those filling-factor values. Having in

hand a value for the aspect ratio of the sample, one can then use the alignment of either the minima (for  $\xi_{\text{fit}} < 1$ ) or the maxima (for  $\xi_{\text{fit}} > 1$ ) with particular filling factors to infer the number of layers. For instance, alignment of the appropriate extrema with filling factors 2, 6, 10, *etc.* implies that the sample is a single layer, whereas alignment with filling factors 4, 8, 12, *etc.* implies that the sample is a bilayer. This type of analysis can be extended to non-rectangular samples; the equivalent rectangle approach appears to work well.

We find for the five samples measured that conductance as a function of gate voltage shows relatively good agreement with theory for short samples ( $L \lesssim 1 \mu\text{m}$ ); in longer samples the best fit aspect ratio differs considerably from the measured sample aspect ratio. We note that using the fit value  $\xi_{\text{fit}}$  for the effective aspect ratio can be more reliable than using the value  $\xi_s$  measured from the micrograph because invisible partial contact can alter the effective aspect ratio.

What could be the physical mechanism of such partial contact? One effect to consider is contact resistance, which would lead to an overall reduction in the experimentally observed values of conductance. In devices fabricated using similar methods to the two-terminal devices in this experiment but with four or more terminals, it is found that contact resistance in the quantum Hall regime at the charge-neutrality point is of the order  $500 \Omega$ , dropping to  $\sim 100 \Omega$  away from charge-neutrality for contacts with similar contact area as the ones used in this experiment. This contact resistance is a small fraction of the resistances measured in the graphene sheet in the quantum Hall regime, hence we rule out the possibility of contact resistance being a main source of discrepancy with theory.

There are scenarios, however, in which contact effects can play a role in altering the aspect ratio. One is that only part of the contact actually injects current, reducing the width causing  $\xi_{\text{fit}}$  to be greater than  $\xi_s$ , as observed in sample A1. Another possibility is that the contacts locally dope the graphene, causing the actual aspect ratio to be smaller. However, for doping to make  $\xi_{\text{fit}} < \xi_s$  in sample B1, it would have to penetrate  $\gtrsim 500 \text{ nm}$  into the graphene, at least two orders of magnitude more than expected [85].

Another, more interesting possibility could be that the picture of an effective medium characterized by local conduction, on which the argument leading up to the semi-circle relation [81] is based, may not hold. This might arise, for instance, from large density fluctuations, giving rise to electron and hole puddles [33] forming a network of  $p$ - $n$  interfaces along which conduction occurs. In this case, the effect of the back gate is to alter the percolation properties of this  $p$ - $n$  network. Magnetotransport across multiple  $p$ - $n$  interfaces cannot be accurately described in terms of a local conductivity model. This situation arises when the distance between contacts is much greater than the scale of disorder, which we take to be  $\lesssim 500$  nm following Ref. [33]. This suggests that samples A1 and B1 should show greater deviation from the present theory than samples A2 and B2, which is indeed the case experimentally. Transport mediated by such states would almost certainly change the conventional picture of local conduction. Further studies are required to clarify the physical mechanism responsible for the observed behavior.

## 5.8 Acknowledgements

Research supported in part by INDEX, an NRI Center, the Harvard NSEC, and the Harvard Center for Nanoscale Systems (CNS), a member of the National Nanotechnology Infrastructure Network (NNIN), which is supported by the National Science Foundation under NSF award no. ECS-0335765. We thank Pablo Jarillo-Herrero for helpful discussions.

## Chapter 6

# Snake States in Graphene p-n Junctions

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We report measurements of the magnetoresistance locally-gated graphene where carriers are injected at and travel parallel to the  $p$ - $n$  junction. In the bipolar regime, a reduction of the longitudinal resistance and enhancement of the transverse resistance are observed, consistent with an additional conduction channel existing at the  $p$ - $n$  interface. This contribution to conductance is studied as a function of perpendicular magnetic field, where the zero-field contribution is found to evolve linearly into peak in the Hall resistance in the quantum Hall regime. Further, an electric field perpendicular to the junction is found to reduce the effect of this interface state in the low-magnetic field regime. A correspondence between this interface state and “snake states” in two-dimensional-electron gases is proposed and its effect on the minimum conductivity in disordered graphene is discussed.<sup>1</sup>

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<sup>1</sup>This chapter is being submitted to Physical Review Letters

## 6.1 Introduction

Graphene is an atomically-thin sheet of carbon atoms arranged into a hexagonal lattice producing a band structure that resembles Dirac fermions. The electron and hole bands meet at a point giving rise to a gapless energy spectrum. In contrast, an energy gap between the electron and hole bands is common in conventional two-dimensional electron gases. The interesting band structure of graphene has led to the prediction of anomalous charge transport properties. Most notably are half-integer values of the quantum Hall (QH) conductance of  $4(n + 1/2) e^2/h$  [11, 52], experimentally observed in Ref. [9, 10], and the finite minimum conductivity  $\sigma_{\min}=4/\pi e^2/h$  [52].

Recently, the ability to control the carrier type locally [40, 47, 74] produced configurations where electrons (*n*-type) and holes (*p*-type) reside spatially adjacent to one another, producing a *p-n* junction (PNJ). The lack of a band gap in single layer graphene permits carriers approaching at normal incidence to access any region near the junction, which is not possible in gapped systems [16]. Bipolar graphene devices have led to the observation of novel conductance quantization in the QH regime [40]. There *p* and *n* type carriers move in edge states in the same direction along the junction and achieve full mode mixing, producing new plateaus in the QH conductance in the bipolar regime [50]. Aside from these locally-gated devices, PNJs play an important role in conduction at the charge-neutrality point (CNP) of disordered graphene samples. At the CNP, the graphene sheet breaks up into an interconnected series of electron and hole puddles [33], a result of the underlying disorder in the sample. In such samples, the PNJs are randomly oriented with respect to the motion of the carrier. Whereas previous studies [40, 47, 74] of locally-gated graphene samples have only investigated transport in geometries where the majority of carriers approach the *p-n* interface at normal incidence, here we report on transport studies where the majority of transport happens parallel to the PNJ.

In this letter, charge transport is studied in a locally-gated graphene PNJ where the *p-n*

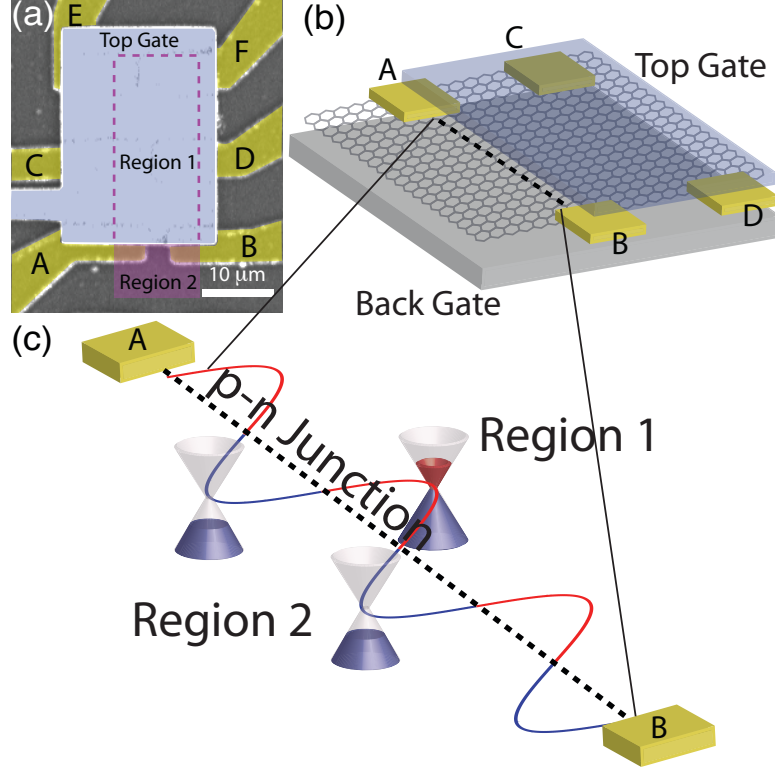


Figure 6.1: (a) Scanning-electron micrograph of a device similar to the one studied here. Electrical contacts A-F (yellow) to graphene (purple) allow for measurements of the quantities  $R_{xx}$ ,  $S_{xx}$ ,  $R_{xy}$ , and  $S_{xy}$  as a function of  $V_{tg}$ ,  $V_{bg}$  and  $B$ . The carrier type and density of Region 1 is controlled by both  $V_{tg}$  and  $V_{bg}$ , while Region 2 is controlled on by  $V_{bg}$ . (b) Schematic of the device. Contacts A and B are partially under and partially outside the top gate. Under certain values of  $V_{tg}$  and  $V_{bg}$ , a p-n junction forms (black dashed line), connecting contacts A and B. (c) Close-up of the PNJ. Modulation of the density across the junction allows for an additional conduction channel to appear between contacts A and B in a magnetic field  $B$ . The change of the Lorentz force (a consequence of the changing sign of the carrier charge) creates a snake-shaped trajectory between the two contacts.

interface connects two electrical contacts to the sample. Using a comparative longitudinal and transverse measurement scheme, a study of transport parallel to the PNJ is performed as a function of top gate ( $V_{tg}$ ), back gate ( $V_{bg}$ ) and perpendicular magnetic field ( $B$ ). It is observed that transport is enhanced in the bipolar regime by states that exist at the interface at all  $B$ , including zero field. Studying the evolution of this enhanced transport into the QH regime, a transition between the low-field states at the PNJ to the high-field edge states is observed. Further,  $V_{bg}$  is used to tune the electric field across the junction and an increase in the electric field results in a decrease in the effect of the interface state

in the low- $B$  regime.

At a PNJ, the density ( $n_s$ ) makes a transition from positively-charged carriers (holes) to negatively-charged carriers (electrons) over a length of order the distance between the graphene sheet and the top gate. The change in the sign of charge produces a change in the sign of the Lorentz force. This creates classical trajectories that are shown in Fig. 6.1(c), resembling snake states observed in inhomogeneous magnetic fields in two-dimensional electron gases [86]. Carriers in these systems are confined to one-dimensional channels and carrier motion occurs in these channels perpendicular to the magnetic field gradient. The density-gradient-induced snake states in graphene PNJs have been predicted in Ref. [87], where it was shown that classical trajectories similar to that of Fig. 6.1(c) can exist at the interface of  $p$  and  $n$  regions.

## 6.2 Devices fabrication and measurement setup

Graphene flakes are obtained via mechanical exfoliation of HOPG on an degenerately-doped Si substrate [5] oxidized by 300 nm of  $\text{SiO}_2$ . Once potential single layer graphene sheets are identified by optical contrast, electrical contacts (5 nm Ti/40 nm Au) are defined and deposited by electron-beam lithography and thermal evaporation. A functionalized-gate-dielectric layer of 30 nm [(TMA +  $\text{NO}_2$ )=2 nm;  $\text{Al}_2\text{O}_3$ =28 nm, see Ref. [40] for details] is grown on top of the graphene sheet and a local gate is deposited in the same manner as the electrical contacts. The doped substrate is used as  $V_{\text{bg}}$  and can control the density globally, while the top gate affects the density only directly under where it is patterned. A completed device, similar to the one used in this study, is shown in Fig. 6.1(a). Importantly, contacts A and B straddle the top gate [Fig. 6.1(b)], so that transport along the PNJ can be studied [Fig. 6.1(c)]. Electrical measurements on two similar devices (measurements from a single device are presented) are performed at a temperature of 4K using a current-bias, lock-in method in  $B$  up to 8T. This device shows QH signatures of single-layer graphene, i.e.,

conductance quantization at  $2, 6, 10 \dots e^2/h$  and has a CNP at  $V_{bg}=40V$ . All measurements presented are taken in the  $V_{bg}$  range of 20V to -40V ( $p$ -type in Region II), where the carrier type is well defined, i.e. at densities larger than the disorder-induced density fluctuations. Similar results were obtained (data not shown) for smaller range of  $V_{bg} > 40V$ .

A comparative measurement scheme is employed to understand how the presence of a PNJ parallel to transport affects conduction. Four-terminal longitudinal [ $S_{xx}=R_{CD,AB}$  where  $R_{ij,kl}$  is a resistance measurement where current is injected at  $i$  and drained at  $j$  and the voltage is measured between  $k$  and  $l$ , Fig. 6.1(a)] and transverse ( $S_{xy}=R_{AD,BC}$ ) resistance measurements along the PNJ are compared to those in which all the contacts are completely under the top gate ( $R_{xx}=R_{CD,EF}$  and  $R_{xy}=R_{CF,DE}$ ). If an additional conduction channel is introduced between contacts A and B [as shown schematically in Fig. 6.1(c)], a *decrease* in  $S_{xx}$  and an *increase* in  $S_{xy}$  should result. A measurement scheme similar to  $S_{xy}$  was employed to study electron focusing in pairs of quantum point contacts (*c.f.* Ref. [88]). Measurements of these four quantities are presented in Fig. 6.2.

### 6.3 Low magnetic field properties of transport along $p$ - $n$ junctions

Measurements of  $R_{xx}$  as a function of ( $V_{tg}$ ) for  $B$  between  $\pm 2T$  [Fig. 6.2(a)] at  $V_{bg}=-20V$  reveal curves commonly observed in unipolar graphene samples [5]. At  $V_{bg}=-20V$ , the entire device consists of  $p$ -type carriers. By identifying the peak in  $R_{xx}$ , a voltage  $V_{tg}^{CNP} \sim 3.5V$  is given to the value of  $V_{tg}$  at which the CNP occurs [indicated as a red dashed line in Figs. 6.2(a-e)] for Region 1. For  $V_{tg} < V_{tg}^{CNP}$ , the entire graphene sheet has a uniform carrier type (but not necessarily density) and is in the unipolar ( $p$ - $p$ ) regime. For  $V_{tg} > V_{tg}^{CNP}$ , a PNJ forms along contacts A-B and the device is in the bipolar regime. A 2D plot of  $R_{xx}(V_{tg}, B)$  [inset of Fig. 6.2(a)] shows that while the resistance increases as a function of  $B$ , the value of the CNP does not change.

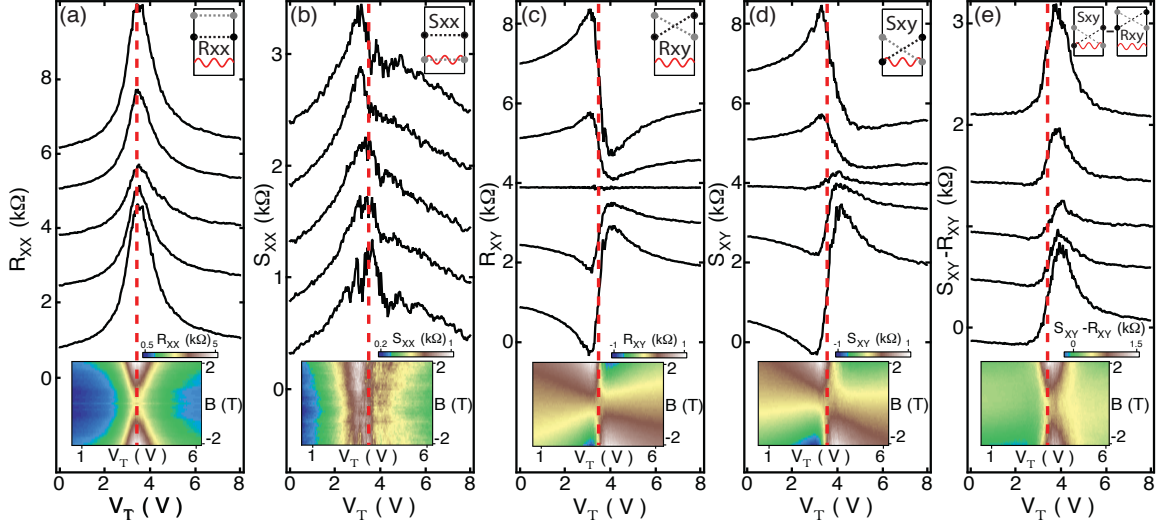


Figure 6.2: Measurements of the four quantities  $R_{xx}$ ,  $S_{xx}$ ,  $R_{xy}$  and  $S_{xy}$  as a function of  $V_{tg}$  (black traces, offset intentional) for  $B$  between  $\pm 2\text{T}$  in  $0.5\text{T}$  steps at a back-gate voltage of  $-20\text{V}$ . The measurement scheme is shown in the upper right inset (black contacts are the current leads and grey are the voltage leads) in each panel. (a)  $R_{xx}(V_{tg})$ . The red dashed line locates the resistance maximum at all  $B$  fields and indicates the CNP for Region 1. Lower inset:  $R_{xx}(V_{tg}, B)$  demonstrating that the CNP does not change over the  $B$  range explored. (b)  $S_{xx}(V_{tg})$ . A drop in resistance of  $0.3 - 0.5\text{k}\Omega$  is observed at the transition from  $p$ - $p$  regime to  $p$ - $n$  regime (red dashed line), indicating that an additional conduction channel has been introduced at the  $p$ - $n$  interface. This resistance drop occurs for the entire  $B$  field range (lower inset). (c)  $R_{xy}(V_{tg})$ . Hall resistance measurement where all the contacts are under the top gate reveals curves that are antisymmetric with respect to the CNP. In contrast,  $S_{xy}$  (d) has larger resistance on the  $p$ - $n$  side of the CNP than  $R_{xy}$ , consistent with an additional conduction channel present at the  $p$ - $n$  interface. This additional amount is quantified in (e) where a plot of  $S_{xy} - R_{xy}$  shows its largest value on the bipolar regime for all  $B$  fields (lower inset).

Measurements of  $S_{xx}(V_{tg})$  for  $B$  between  $\pm 2\text{T}$  [Fig. 6.2(b)] at  $V_{bg} = -20\text{V}$  produce resistance traces that are different from  $R_{xx}$  and longitudinal measurements of previous graphene PNJ. Here, as the PNJ is form, there is a marked decrease in resistance of  $\sim 0.3\text{k}\Omega$ , producing a resistance curve that is *lower* on the  $p$ - $n$  side of the CNP. This decrease in resistance happens even at  $B=0\text{T}$ . The opposite effect is observed in PNJ - where carriers approach the junction at mostly normal incidence - creating an increase in resistance [40, 47] in the bipolar regime. The inset of Fig. 6.2(b) indicates that this drop in resistance persists throughout the entire low- $B$  field range.

$R_{xy}(V_{tg})$  traces [Fig. 6.2(c)] at  $V_{bg} = -20\text{V}$  for  $B \pm 2$  are similar to those for single-gate

graphene [5] in the low  $B$ -field regime. As the CNP is crossed  $R_{xy}$  changes sign, indicating a change in carrier type ( $p \rightarrow n$ ) as a function of  $V_{tg}$ . These curves are antisymmetric with respect to the CNP and  $B$  [see black curves and lower inset of 2(c)]. By comparison, this is not the case for  $S_{xy}$  [Fig. 6.2(d)]. The resistance curves there are not antisymmetric and have resistance values greater on the  $p$ - $n$  side ( $S_{xy}^{p-n} > R_{xy}^{p-n}$ ). This increase in resistance is quantified in Fig. 6.2(e), where a plot of the difference,  $S_{xy} - R_{xy}$ , is consistently larger in the  $p$ - $n$  regime for the entire low  $B$ -field range [inset of Fig. 6.2(e)]. The increase in  $S_{xy}$  occurs even at  $B=0T$  at a value of  $0.5k\Omega$  and persists in for a range of  $\sim 1V$  in  $V_{tg}$ , while  $R_{xy}$  shows no systematic change in resistance. At larger  $|B|$  this difference increases, reaching a value of  $1.5k\Omega$  at  $B=\pm 2T$ .

## 6.4 $S_{xy}$ in the quantum Hall regime

Measurements of  $S_{xy}$  were carried out in the QH regime, where current is carried entirely by one-dimensional edge channels.  $S_{xy}(V_{tg})$  in the unipolar regime shows the typical QH effect for graphene, producing quantized conductance values of 2, 6 and  $10 e^2/h$  [Fig. 6.3(a), left of the red dashed line]. Once in the  $p$ - $n$  regime [Fig. 6.3(a), right of the red dashed line], the quantization plateaus disappear and a series of peaks develop in the resistance. The voltage at  $V_1$  and  $V_2$  [Fig. 6.3(b)] are

$$eV_1 = \mu_s; \quad eV_2 = \frac{|\nu_{R2}| \times \mu_s + |\nu_{R1}| \times \mu_d}{|\nu_{R1}| + |\nu_{R2}|} \quad (6.1)$$

where  $\nu_{R1}(\nu_{R2})$  is the filling factor of Region 1(Region 2) and  $\mu_s(\mu_d)$  is the chemical potential of the source(drain). Using these values at  $V_{bg}=-20V$  ( $\nu_{R1}=2$ ,  $\nu_{R2}=10$ ), the Hall resistance at  $B=8T$  should be reduced from  $h/2e^2$  to  $(V_2 - V_1)/I \sim -2k\Omega$ , which is approximately the resistance observed for  $S_{xy}$  in the bipolar regime [Fig. 6.3(a)]. In addition to the reduction of resistance, a peak in resistance appears at  $V_{tg}=5.5V$  at  $8T$  [Fig. 6.3(a), indicated by black arrow] of magnitude  $\sim 2k\Omega$ . The peak in resistance corresponds to the transition of filling factor in Region 1 ( $\nu_{R1}=2 \rightarrow 6$ ), suggesting that the peak is due to contributions the

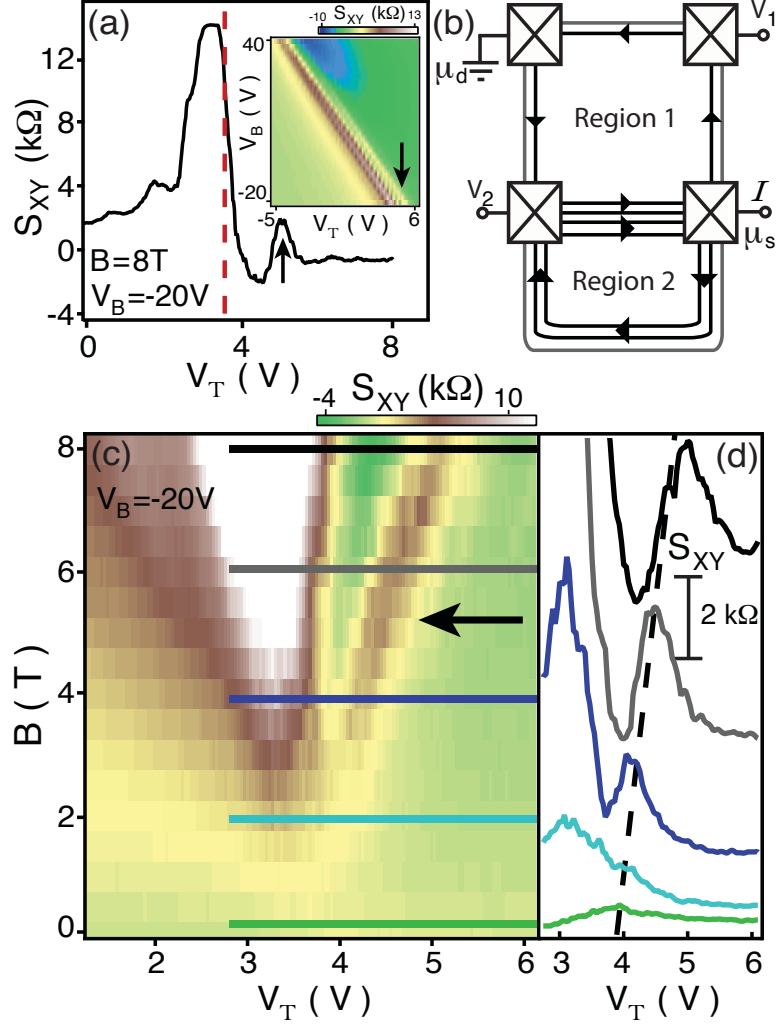


Figure 6.3: (a)  $S_{xy}(V_{tg})$  at  $B=8T$  shows well developed QH plateaus of 2, 6 and  $10 e^2/h$  in the unipolar regime. The resistance is lower in the  $p-n$  regime (for values of  $V_{tg}$  on the right of the dashed red line), a result of edge state transport in Region 2. A peak in resistance (indicated by the black arrow) develops on the bipolar side. Inset: This peak (yellow line indicated by the black arrow) is reduced in magnitude as  $V_{bg}$  approaches the CNP ( $V_{bg}=40V$ ) of Region 1. (b) Schematic of the edge states present in the two regions of the device. When the edge states propagate as shown, the voltage difference between  $V_1$  and  $V_2$  is reduced. (c)  $S_{xy}(V_{tg}, B)$  for  $B$  between 0 and 8T. In addition to this reduction in resistance, a peak forms that moves linearly in the  $(V_{tg}, B)$  space. (d) horizontal cuts corresponding to the colored lines in Fig. 6.3(c) show a gradual evolution (black dashed line) of the zero  $B$ -field peak to the resistance peak in the QH regime.

resistance from  $\rho_{xx}$ . This case is unlikely as the contribution from  $\rho_{xx}$  in the  $p-p$  regime is not as large as this peak observed in the  $p-n$  regime. The reduction of resistance and peak disappear as the CNP of Region 1 is approached [inset of Fig. 6.3(a)].  $S_{xy}(V_{tg}, B)$

reveals that this peak (black arrow) moves linearly away from the CNP of Region 1 as  $B$  is increased [Fig. 6.3(c)]. One-dimensional cuts of  $S_{xy}(V_{tg}, B)$  [Fig. 6.3(d)] in the  $p$ - $n$  region demonstrate that the zero-field peak in the transverse resistance  $S_{xy}(B = 0T)$  gradually evolves into the peak in the QH regime, suggesting that these phenomena have similar origins.

## 6.5 $V_{bg}$ dependence of the snake state

The  $V_{bg}$  dependence of the peak resistance in  $S_{xy}-R_{xy}$  is shown in Fig. 6.4, plotted for five different  $B$  between 0 and 2T, in 0.5T increments in the  $V_{bg}$  range of 20V to -40V (black lines are guides to the eye). It is found that the position of the peak moves linearly in the  $(V_{tg}, V_{bg})$  space (data not shown) but decreases as the magnitude of  $V_{bg} - V_{bg}^{CNP}$  is increased, i.e. as the electric field perpendicular to the junction increases. The change in resistance gets stronger for increases in the  $B$  field, changing  $\sim 0.2k\Omega$  at  $B=0T$  to  $\sim 1k\Omega$  at  $B=2T$  over the  $V_{bg}$  range shown here.

## 6.6 Discussion

What could be a possible origin for this increased conduction channel provided by the PNJ? In the QH regime, the conduction along the PNJ is provided for by the counter-propagating edge states in the  $p$  and  $n$  sides of the junction. The change in sign at the interface allows for snake state propagation along the junction [87], enhancing conductance. The formation of the snake states takes place at a  $B > B_\star = \hbar\sqrt{\pi n_S}/eB$  [16, 87]. At the  $p$ - $n$  interface, where the density  $n_S$  goes from positive to negative values (i.e. through  $n_S=0$ ), this condition can always be met, suggesting that formation of Landau-level-like edge states can exist even at  $B=0T$ . The behavior, however, of  $B_\star$  as  $B \rightarrow 0T$  and  $n_s \rightarrow 0$ , is not currently understood. If a Landau-like level did form, an additional conductance channel with resistance of order  $h/2e^2=12.9k\Omega$  would appear. In the QH regime, this would

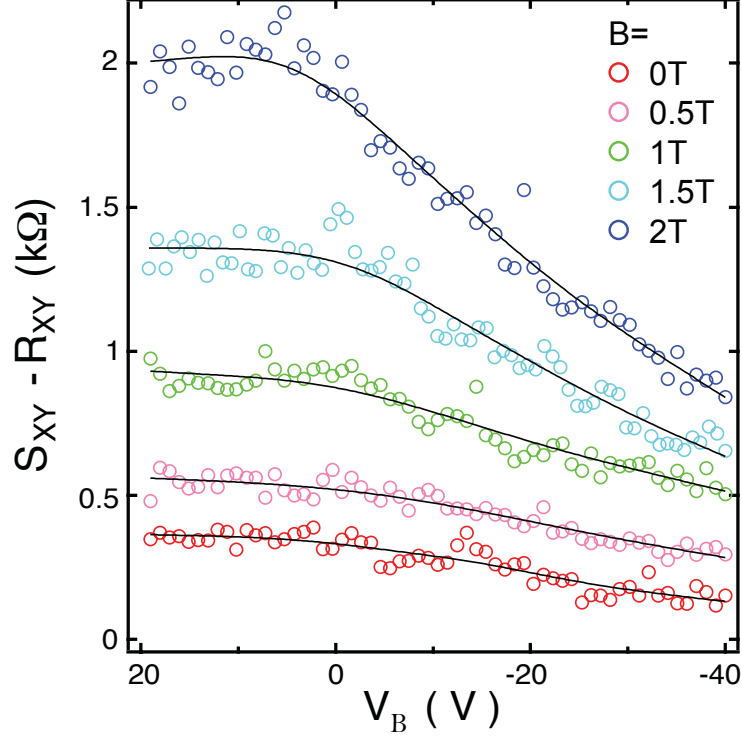


Figure 6.4: Back-gate voltage dependence of the difference  $S_{xy}-R_{xy}$  for  $B$  between 0 and 2T in 0.5T increments.  $S_{xy}-R_{xy}$  is reduced as the difference  $|V_{bg}-V_{bg}^{CNP}|$  becomes larger for all  $B$  fields. Solid black lines are guides to the eye. The decrease in resistance in this  $V_{bg}$  range increases as the perpendicular field is increased, rising from  $\sim 0.2\text{k}\Omega$  at  $B=0\text{T}$  to  $\sim 1\text{k}\Omega$  at  $B=2\text{T}$ .

be the only mode of transport, as the bulk is localized, and the resistance would be exactly  $h/2e^2$ . For small  $B$ , the bulk is not localized. If we take the added conduction channel as adding in parallel with the bulk resistance ( $\sim 1\text{k}\Omega$ ), the resulting change in resistance would be  $(12.9 \times 1)/(12.9 + 1)\text{k}\Omega \sim 0.1\text{k}\Omega$ , which is about the resistance drop observed in Fig. 6.2(b). The observed reduction of this phenomena with increase  $V_{bg}$  (Fig. 6.4) may be due to the incomplete mixing of edge states observed for higher Landau levels, resulting in a destruction of the quantized conductance plateaus, as was observed in Ref. [40]. A more interesting interpretation would be the collapse of the Landau levels at higher perpendicular electric fields [89]. If this phenomena is a result of Landau-level-like edge modes, the low  $B$  fields in which it is observed should allow for experimentally realizable electric fields to collapse the Landau-levels completely, removing the additional conduction channel completely.

If the  $p$ - $n$  interface is providing an additional channel for conduction, this would be an important contribution to the measured  $\sigma_{\min}$ , where many PNJs are present. Charge transport in disordered graphene samples has been studied experimentally [9, 34] and theoretical predictions have been made for  $\sigma_{\min}$  [35, 36], however consensus has yet to be reached. Taking into account the resistance of the PNJs and appropriate values for the size of density fluctuations, a value  $\sigma_{\min} \sim 2.5e^2/h$  was obtained, 2 to 6 times lower than the experimentally reported values [9, 34]. The additional conduction along the interface could be a source conductance that raises this theoretical value to those closer to the experimentally measured values.

## 6.7 Acknowledgements

We thank L. S. Levitov and D. A. Abanin for useful discussions. Research supported in part by INDEX, an NRI Center, and Harvard NSEC.

## Chapter 7

# Precision Etching of Graphene with a Helium Ion Beam

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We report on the use of a helium ion microscope as a potential technique for precise nanopatterning of graphene films. Combined with an automated pattern generation system, we demonstrate controlled etching and patterning of graphene, giving precise command over the geometry of the graphene nanostructure. After determination of suitable doses, sharp edge profiles and clean etching of areas when cutting layers of graphene were observed. This technique could be an avenue for precise materials modification for future graphene based device fabrication.<sup>1</sup>

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<sup>1</sup>This chapter is being submitted to Nano Letters.

## 7.1 Introduction

Helium Ion Microscopy (HeIM) has been introduced as an ultra high-resolution imaging technology for a variety of materials applications, with unique contrast mechanisms and imaging abilities [90]. The HeIM has been developed primarily as an imaging tool. However, being a charged ion beam instrument it is also possible to perform milling and sputtering tasks more commonly associated with a conventional gallium ion beam systems (FIB). One advantage is the ability to mill and sputter soft materials with extremely low rates. The Helium ion microscope also has been shown to have an extremely small probe size in the order of 0.5 nm or better [91]. The combination of these features has the capability to make this instrument one of the most precise direct fabrication tools currently available for materials, especially for low-z materials, for example graphene layers.

Graphene is a two-dimensional carbon-based crystal that has only recently been discovered experimentally [5]. It is desirable for many experiments and potential applications involving graphene that it is patterned at the nanoscale. Lithography-based nanostructuring methods reported thus far include electron beam lithography in conjunction with reactive ion etching ([21, 22, 92]) and direct etching with a focused electron beam in a transmission electron microscope (TEM) [93]. Both methods are suitable to produce patterns in the tens of nanometer range. While the former is limited by random underetching effects in oxygen plasma, the latter relies on transferring graphene flakes onto TEM grids, which is not suitable for larger scale fabrication of devices. This work focuses on process considerations of He ion etching of graphene, while specifics of graphene field effect transistors are reported elsewhere [94].

## 7.2 Helium ion beam process considerations

The design principle of HeIM is based on the field ion microscope operating in a UHV environment with a cryogenically cooled sharp tungsten tip, to which He ions are introduced

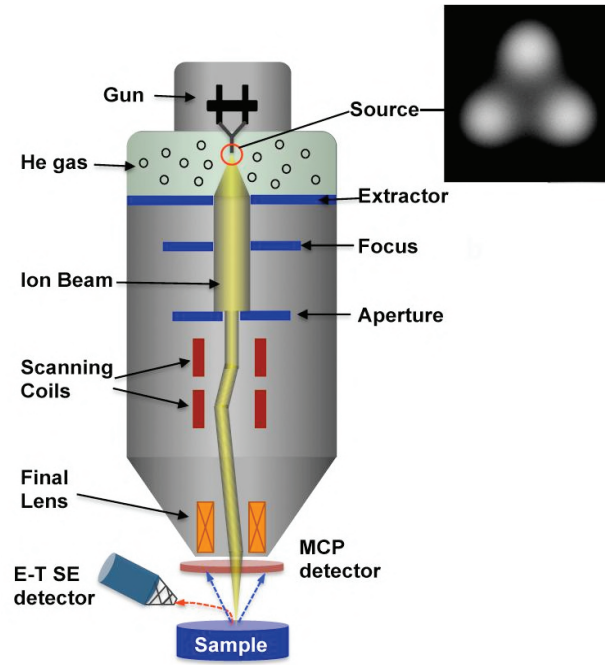


Figure 7.1: Schematic of a graphene device. Inset: Photograph of the microscope chamber with installed chip.

(Fig. 7.1). The tip is manufactured in such a way that it is truncated by a trimer of atoms (inset of Fig. 7.1); the gun is centered in such a way that only a single atom emission is used for imaging. The beam current can be modified by changing the imaging gas pressure, with typical operation in the range of fA to pA. The exact details of the microscope operation have been described elsewhere [91].

The physical interactions of the ion beam with the sample are critical to determine the ultimate spot size for the highest possible resolution; it also ultimately controls the quality of the generated ion etched pattern when combined with sample proximity effects. Typical beam/specimen interactions in HeIM and the variety of resulting signals and emitted particles are indicated in the schematic in Fig. 7.2.

The size of the ion-interaction volume in the substrate material depends on the elemental composition and density of the material and on the acceleration voltage applied to the

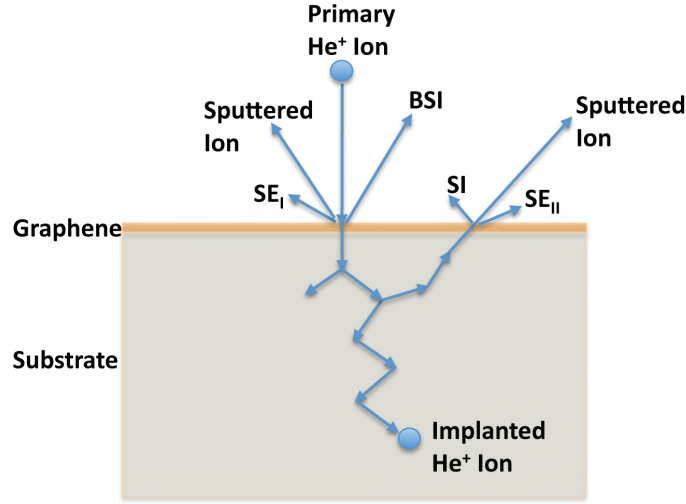


Figure 7.2: Schematic of the interactions of primary energetic He ions with a graphene layer on SiO<sub>2</sub> substrate.

ion source. The primary advantage for HeIM that can be utilized for etching graphene layers is that the interaction volume of the Helium ion is intrinsically smaller than in a typical scanning electron beam or a FIB at the corresponding accelerating voltage. The ion interaction volume in the top few nm of the material being the determining factor for ultimate patterning resolution of graphene. TRIM calculations [95, 96] have been used to simulate ion beam propagation and average sputtering yield in graphene on substrates. Simulation for gallium ions for a graphene film on a typical substrate of 285 nm SiO<sub>2</sub> on silicon is shown in Fig. 7.3a. The heavy ions deposit the majority of their kinetic energy in the upper most parts of the material. While this makes them highly effective at milling and etching, the resulting surface region interaction volume limits the possible feature size to values far larger than the actual beam diameter.

TRIM calculations for helium ions on an identical specimen, in contrast, show that

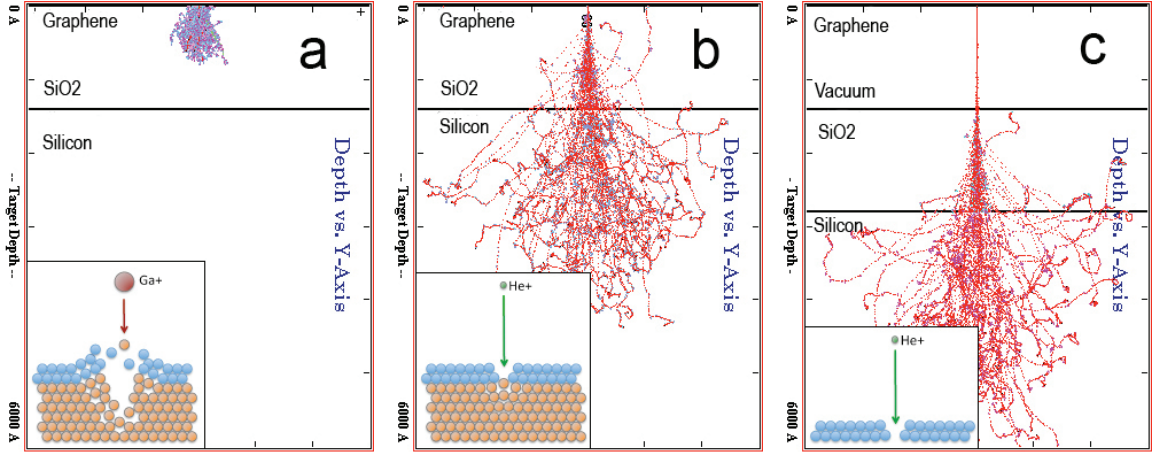


Figure 7.3: TRIM simulations comparing a) 30 kV Ga ions and b) 30kV He ions for range and trajectory in graphene layers on SiO<sub>2</sub> on silicon substrate. c) Range and trajectory of 30 kV He ions through a suspended graphene layer over vacuum, SiO<sub>2</sub> and silicon substrate. (Insets) Schematic comparison between Ga<sup>+</sup> ion and He<sup>+</sup> ion interaction with graphene samples from molecular dynamics simulations [96].

99.6% of the ions pass directly through the graphene with no ion interaction at all. Instead, the majority of the ion energy is deposited deep within the silicon substrate (Fig. 7.3b). The helium ions lighter mass and higher speed results in smaller interaction volume with the surface layers and hence in better resolution and potential milling feature size. From the perspective of sputtering and patterning, the result is a reduced proximity effect in the surface layer. The light ion mass results in low energy transfer and hence a relatively lower sputtering yield compared to gallium.

Figure 3c shows the situation for a suspended layer of graphene over SiO<sub>2</sub> and silicon substrate. The thickness of the vacuum gap and the SiO<sub>2</sub> add up to 285 nm, as would be the case in a device fabricated from a typical substrate as in Fig. 7.3b. In this case, there is little to no observable backscattering to the graphene layer. This suggests suspended graphene as an ideal substrate for resolution tests of helium ion etching. In addition, the lack of interaction of backscattered ions with the graphene film should make suspended devices particularly suitable for He ion etching.

Based on the TRIM calculations the milled line width for helium ions compared with

gallium ions is about a factor of 10 smaller. Gallium ions also could leave ionic contamination in samples which would be problematic for graphene devices, were as the helium ions do not appear to present issues as severe. An important result from these simulations is the indication that the lack of helium ion beam divergence in the vicinity of the surface of the sample down to a depth of about 100 nm should enable nanometer scale fine etching and cutting. Following from molecular dynamics [96] a schematic can be constructed to detail the collision cascade a form of proximity effect during ion bombardment that shows clearly the differences between using gallium ions and helium ion bombardment for milling and etching (Insets in Fig. 7.3).

### 7.3 He ion beam microscope

The helium ion microscope imaging and etching was done using the ORION™ helium ion microscope (Instrument Serial #4) manufactured by Carl Zeiss SMT. The instrument was operated at 30kV acceleration voltage with a measured beam current of 1 pA to 1.6 pA. While hydrocarbons have been used previously to write patterns onto graphene [97], here avoiding contamination in the instrument is critical to producing a clean working result. As such the HeIM chamber is cleaned with air plasma overnight prior to sample patterning. This is performed using an Evactron type plasma cleaner attached to the chamber with a cycle time of 15 minutes on and 45 minutes off for a minimum of 10 cycles at 12 Watts power [98].

A commercial pattern generation system (Nanometer Pattern Generation System, NPGS) was installed on the HeIM in order to perform controlled etching of the samples using a variety of conditions. The NPGS system allowed for dose variations, the use of random patterns and pattern alignment to existing structures (i.e. devices [94]).

Test writing was performed on 285 nm-thick SiO<sub>2</sub> on a Si substrate. Initial dose exposures indicated a dose of 1.2 nC/cm as an optimal initial setting for ion beam and dwell

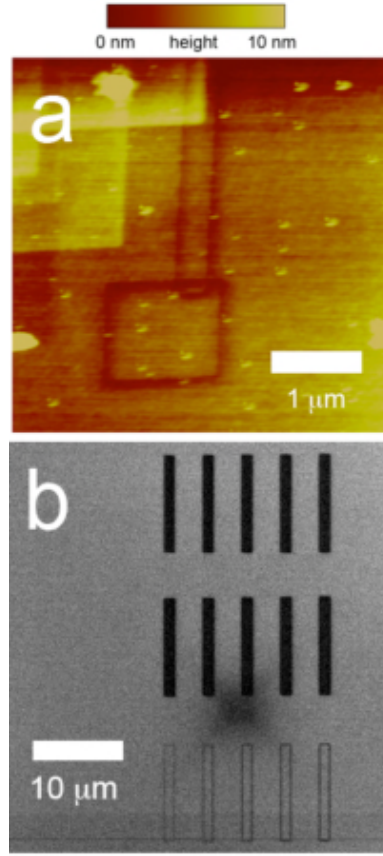


Figure 7.4: a) Test patterns written into a 285 nm SiO<sub>2</sub> film on silicon substrate as measured with AFM and b) showing etching of boxes and line box patterns.

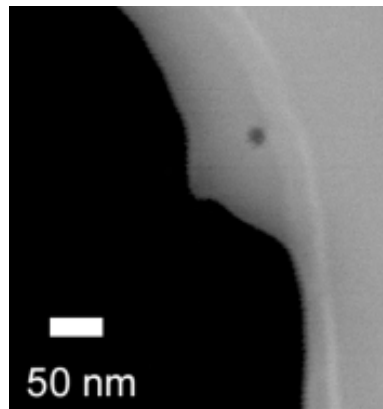


Figure 7.5: HeIM image of a hole etched into a multi layer graphene film (grey) on a SiO<sub>2</sub> substrate (black)

times in the pattern generation system. AFM and HeIM images [Fig 4(a,b)] shown sharp, well-defined patterned etched in SiO<sub>2</sub>.

Graphene flakes were then deposited onto the SiO<sub>2</sub> by mechanical exfoliation, similar

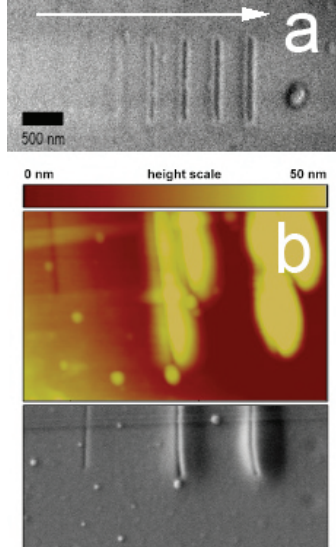


Figure 7.6: a) HeIM image of a dose variation test pattern in graphene, lower to higher dwell times represent increased helium ion doses. b) AFM image with corresponding SEM image of a pattern etched with 20, 100 and 200 nC/cm line dose variation (from left to right).

to the method described in Ref. [5] with the modifications of the process as described in Ref. [40]. Next, mono- and multi-layer graphene flakes were identified with an optical microscope.

## 7.4 Results and discussions

In an initial experiment, the He ion beam was focused on freestanding graphene flakes, resulting in small holes in the material. Fig. 7.5 shows a HeIM image of one such hole with a diameter of 15 nm. Variations of this dose were performed to ascertain the optimal operation point for He ion etching. Fig. 7.6a shows a HeIM image of lines etched in graphene sample, showing changes in the pattern with increasing beam dose from left to right at a measured probe current of 1.6 pA. The dose was varied from 3 nC/cm to 15 nC/cm in 3 nC/cm steps. The result indicates that a suitable dose for etching a graphene sample with the HeIM/NPGS settings used in this work is in the range of 10-15 nC/cm. A larger dose variation performed with 20, 100 and 200 nC/cm is shown in Fig. 7.6b. The SEM image

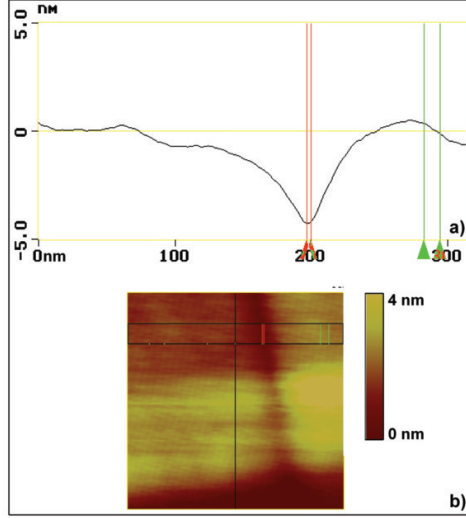


Figure 7.7: a) AFM step profile analysis for the graphene cut in Fig. 7.6b with a dose rate of 20 nC/cm resulting in a depth of 4 nm. b) AFM image used for the step profile. The profile was taken along the upper part of the image, indicated by the two black lines.

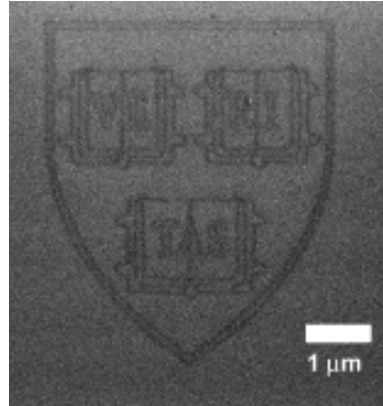


Figure 7.8: HeIM image of a high resolution Harvard University logo etched into multi-layer graphene.

shows that all doses lead to a cut in the graphene layers. However, the combination of SEM and AFM images further reveals that for very high doses the underlying substrate can swell up by at least 50 nm from the effect of ion knock-on damage to the underlying silicon. The detailed AFM analysis for the graphene cut with the low dose rate of 20 nC/cm for test lines resulted in a measured depth of 4 nm (Fig. 7.7).

In principle, the pattern generation system allows etching of any pattern in graphene.

This is demonstrated in Fig. 7.8 with a Harvard University logo etched into multi-layer graphene with line widths well below 50 nm. The overall dimensions of the logo are about  $4\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$ .

## 7.5 Conclusions

We have successfully shown that it is possible to precisely cut, etch graphene with 30kV helium ions and have shown results for the patterning of single and multiple layers of graphene. In conjunction with a pattern generation system the helium ion microscope can be routinely used to pattern graphene. This research may lead to graphene nanoscale electronic devices that take advantage of the semi-conducting properties and physics of nanoscale shaped graphene.

## Chapter 8

# Etching of Graphene Devices with a Helium Ion Beam

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We report on the etching of graphene devices with a helium ion beam. The etching process can be used to nanostructure and electrically isolate different regions in a graphene device, as demonstrated by etching a channel in a suspended graphene device with etched gaps down to about 10nm. Graphene devices on SiO<sub>2</sub> substrates, etched with lower He ion doses, are found to have a residual conductivity after etching. We attribute this effect to hydrocarbon contamination.<sup>1</sup>

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<sup>1</sup>This chapter is being submitted to App. Phys. Lett.

## 8.1 Introduction

Graphene, a thermally stable two-dimensional carbon-based crystal, has attracted an immense research interest as both a model system for fundamental physics as well as for nanoelectronics applications [5, 7]. Many experiments in the field are targeted at graphene films or devices where artificial confinement in one or two dimensions produces nanoribbons or quantum dots. Typically, such structures are on the order of 5 to 50 nanometers and have been fabricated either by electron beam lithography and reactive ion etching ([21, 22, 92, 99]), by chemical derivation, including cutting of carbon nanotubes ([19, 20, 100]). While both methods are suitable to produce devices near the atomic limit, they also have shortcomings. Reactive ion etching typically involves oxygen plasma, which tends to underetch the resist masks randomly, creating very disordered edges. Chemical derivation methods are limited in that they result in randomly shaped and distributed flakes and devices. It has further been proposed to etch graphene at the nanoscale with a focused electron beam [93]. This method, however, requires suspending graphene on specific transmission electron microscope grids, making it difficult to perform electrical measurements.

Helium Ion Microscopy (HeIM) has recently been introduced as an ultra-high-resolution imaging technology for nanostructures and materials [90, 91, 101]. In this work we use a helium ion microscope (“Orion, Carl Zeiss SMT) as a tool to modify properties of graphene devices in a controlled manner. The HeIM is particularly well suited for this purpose because it produces a high-brightness, low-energy-spread, sub-nanometer size beam. The microscope benefits from the ultra short de Broglie wavelength, which is approximately 100 times smaller than the corresponding electron wavelength. This gives the beam an ultimate resolution of 0.5nm or better [91], making it a highly attractive tool for precision modification of graphene devices. While process details are published elsewhere [102], this letter focuses on the modification of device properties of graphene.

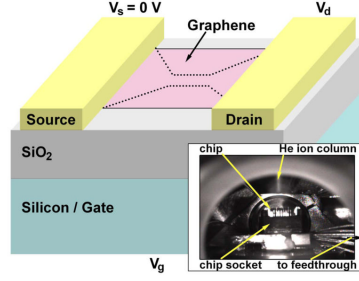


Figure 8.1: Schematic of a graphene device. Inset: Photograph of the microscope chamber with installed chip.

## 8.2 Experimental setup

Graphene was deposited onto  $\sim 300$  nm of silicon dioxide on degenerately doped silicon by mechanical exfoliation [40], similar to the method described in Ref. [5]. Next, mono- and few layer graphene flakes were identified with an optical microscope. Contacts to the graphene were defined by electron beam lithography, followed by evaporation of chromium/gold (3 nm/150 nm) and titanium/gold (5 nm/40 nm). Suspension of the graphene sheet was obtained by wet etching of the underlying SiO<sub>2</sub> in diluted HF, followed by critical point drying. All devices were measured in a standard graphene transistor configuration, with the evaporated contacts acting as source and drain, and the highly doped silicon substrate as a (back-) gate electrode (Fig. 8.1a). The drain current  $I_d$  through the flake is then measured as a function of gate voltage  $V_g$  for a constant drain voltage  $V_d$ . Electrical data of suspended devices were taken before and after He ion etching with two Keithley 2400 source meters in a Lakeshore probe station at a pressure of  $5 \times 10^{-3}$  mbar. The second set of graphene devices on SiO<sub>2</sub> substrate were wirebonded to chip carriers and placed in a chip socket inside the Helium ion microscope to enable in-situ electrical measurements (inset in Fig. 8.1). These were taken at a pressure of  $1 \times 10^{-6}$  mbar with an Agilent 4155B parameter analyzer connected to the device via a vacuum feedthrough. All measurements were taken at room temperature.

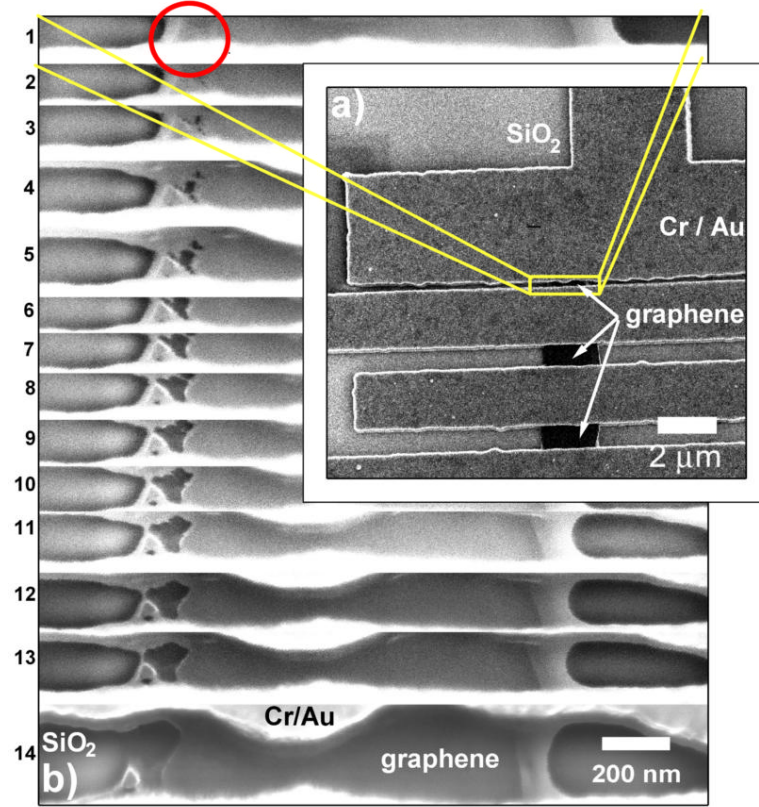


Figure 8.2: a) HeIM image of suspended graphene devices. The yellow box indicates the area that was subsequently imaged and etched. The red circle indicates the area where etching occurred initially (color online). b) Sequence of images of progressive etching of a suspended graphene sheet.

### 8.3 Results and discussion

A suspended graphene device with a length of  $\sim 150$  nm and a width of  $\sim 1.5$   $\mu\text{m}$ , shown in the HeIM microscope image in Fig. 8.2a, was He ion etched by sequential imaging in high resolution. The graphene was exposed to the He ion beam at a field of view of  $2$   $\mu\text{m}$  x  $2$   $\mu\text{m}$  and an image size of  $2048 \times 2048$  pixels, which resulted in a pixel spacing of  $\sim 1$  nm. The dwell time was chosen to be  $50$   $\mu\text{s}$  resulting in an effective line dose of  $0.8$  nC/cm. Fig. 8.2b shows a sequence of images taken under these conditions (1-14). The red circle

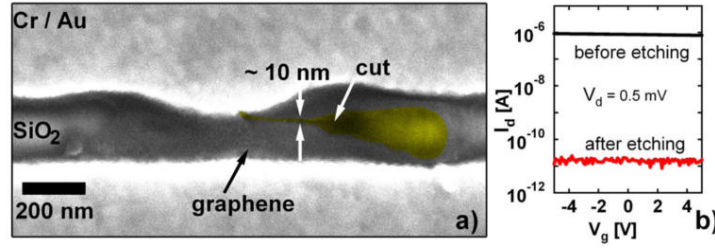


Figure 8.3: a) HeIM image of a suspended graphene device after etching with minimum feature sizes of about 10 nm. b) Electrical measurement of the device before and after etching.

indicates the region of the graphene flake where etching occurred initially. Each scan with the He ion beam resulted in an increase of etched area. After thirteen scans, the dwell time, and hence the image quality, was increased to 500  $\mu$ s, equivalent to a line dose of 8 nC/cm, still not sufficient to complete etch the device (Fig. 8.2 scans 1-14). These images indicate that removal of edge atoms is favorable over atoms within in the graphene crystal. The remaining graphene film was etched using live scanning mode with a 100 nm to 10 nm field of view. Here, etching was confirmed via the live screen image. A resultant cut with minimum feature sizes in the 10 nm range is shown in the HeIM image in Fig. 8.3a. The gap was measured with DesignCAD software after importing the original image.

After etching a trench across the entire graphene flake, the device was removed from the He ion microscope and its drain current was measured as a function of back gate voltage (Fig. 8.3b,  $V_d = 0.5$  mV, note that the gate voltage range is limited in suspended graphene devices [103], and hence  $I_d$  changes little with  $V_g$ ). The current dropped to about 15 pA, compared to 1  $\mu$ A prior to etching. While the latter is typical for a functional graphene device of the given dimensions, the post-etching value corresponds to the noise level of the measurement setup. Adjacent, non-imaged devices made from the same graphene flake showed conductivity similar to the investigated device prior to imaging. These results confirm that the graphene was etched successfully using the He ion beam.

Next, the drain current of a graphene device on SiO<sub>2</sub> substrate was measured inside

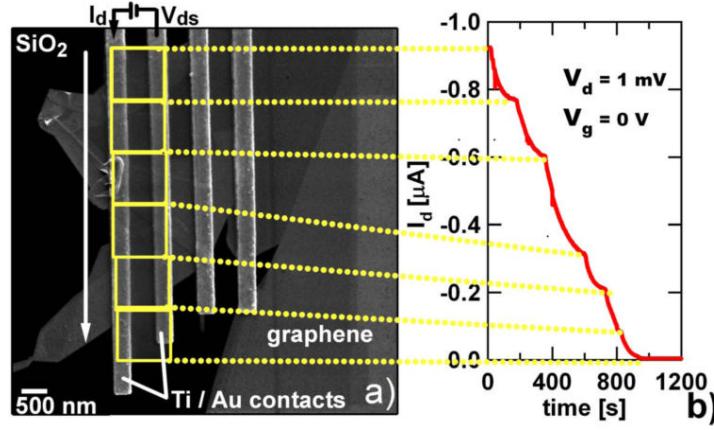


Figure 8.4: a) HeIM image of a graphene device. The boxes indicate the field of view used for etching. The window was subsequently moved in the direction of the arrow. b) Drain current vs. time of exposure of the graphene device. The etching window was moved as the current saturated.

the He ion microscope while part of it was exposed to the ion beam. A field of view of  $1 \mu\text{m} \times 1 \mu\text{m}$  was chosen, indicated by the yellow box in Fig. 8.4a. After about 150 seconds the current saturated, indicating complete etching of the graphene inside the field of view (Fig. 8.4b). At this point the imaging window was moved to the next part of the device in the direction of the white arrow in Fig 4a. The current was again monitored until it saturated. A beam current of 1 pA, dwell time of  $3 \mu\text{s}$ , and pixel spacing of 1 nm allowed us to estimate a suitable He ion line dose for etching graphene on SiO<sub>2</sub>: 1.5 nC/cm. A residual drain current of about 4 nA was measured after etching the entire device, which could not be reduced further by subsequent He ion beam exposure. We attribute this residual conductivity to contamination of the SiO<sub>2</sub> surface with hydrocarbons.

## 8.4 Conclusions and acknowledgements

We demonstrated etching of graphene devices with a helium ion beam for the first time. Suspended graphene has been etched conclusively, with minimum feature sizes in the 10 nm range. Graphene on SiO<sub>2</sub> was etched with a lower dose compared to suspended graphene. However, these devices showed a residual conductivity attributed to contaminants on the

surface. Helium ion etching can be considered an alternative nanofabrication method for suspended graphene devices and, if contamination issues can be solved, graphene on SiO<sub>2</sub> substrates.

MCL gratefully acknowledges the support of the Alexander von Humboldt foundation through a Feodor Lynen Research Fellowship. The authors thank S. Nakaharai for fruitful discussions regarding the process.

## Appendix A

# Graphene Deposition by Mechanical Exfoliation

This section describes the art of graphene deposition. This method has changed substantially since I started trying to do this in 2005 (compare the method described here to the one used in the Supplementary Material of chapter 3 on  $p$ - $n$  junctions in the Quantum Hall Regime). The current method has been the most fruitful, quantified by the number and area of the resulting graphene flakes, but I'm sure that the method could be further improved and honed. The starting material is very important. I've heard stories of professors traveling to obscure, foreign places to try and find the highest quality graphene. The time constraints of graduate school preclude such excursion, but fortunate I've had luck with commercially available graphite. Graphite crystals were obtained from SPI supplies ([www.2spi.com](http://www.2spi.com)). A variety of sample sizes and quality is available and highly ordered pyrolytic graphite (HOPG) works the best. Many grades are available (see <http://www.2spi.com/catalog/new/hopgsub.php>) and I started off using SPI-1 Grade (5mm  $\times$  5mm). I have since found that, although more expensive, the ZYA grade [Fig. A.1(a)] produces the largest flake size. The size and lot number of our graphite source used for the most recent experiments is HOPG ZYA 12x12x2mm Lot #1130605, shown in Fig. A.1(b).

The zeroth step is to go in the cleanroom, all this should be done in a clean environment. The first step in mechanical exfoliation is to cleave the graphite crystal with tape. I have used a variety of tape types, mainly to attempt to remove the residual contamination left by the tape. For example, water-soluble and blue cleanroom tape were each staples of this method for a long time. I have found that, if done correctly, use of standard Scotch<sup>TM</sup> gives the largest flake size and does not contaminate the graphene. Cleaving the graphite is performed by pressing the tape with a gloved finger over the graphite. Rub plastic-tipped tweezers over the graphite to ensure that the tape is pressed firmly against the surface [Fig. A.2(a)]. Next, peel the tape off the graphite [Fig. A.2(b)]. A square of roughly the same lateral dimensions of the graphite should be stuck to the tape. Take another piece of tape and press it against the piece of tape used to cleave the graphite, with the graphite side up. Rub your tweezers over the tape-graphite-tape sandwich until the two pieces of tape

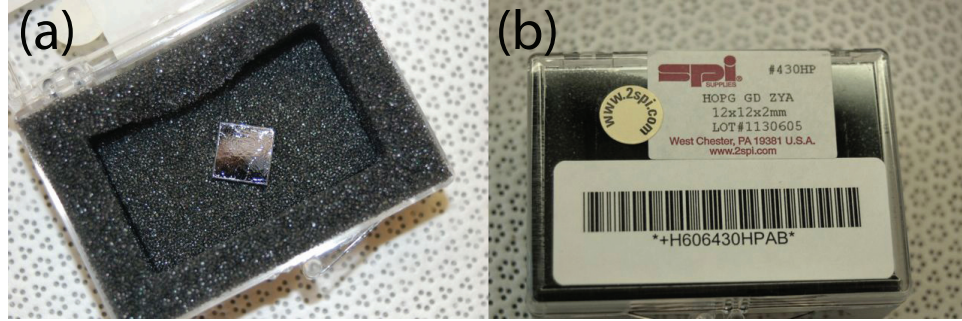


Figure A.1: (a) a picture of the ZYA-grade graphite material currently used in the Marcus Lab to produce graphene. (b) Size, quality and Lot Number of the graphite.

are pressed firmly together [Fig. A.2(c)]. Take the tape on the left hand side of Fig. A.2(d) and use a fresh piece of tape to make another tape-graphite-tape sandwich. With these two pieces of tape, repeat the press and peel process several ( $\sim 10$ ) times until the piece of tape covered in smaller, faint grey graphite islands, as shown in Fig. A.2(e). It is important that the area of the tape that will be placed on your oxidized Silicon chip is completely covered with these faint, grey islands. This helps to prevent transfer of tape residue to the graphene or substrate surface.

Next, get a chip comprised of  $\sim 285$  nm of  $\text{SiO}_2$  on a degenerately doped Silicon wafer. Wafers were obtained from Nova Electronic Materials (<http://www.novawafers.com/>). Not all oxides are created equal. The samples deposited on the flattest oxides seem to have, on average, higher mobilities. The flattest oxides are produced by thermal growth of a *dry* oxide. Dry oxide means that there is no water vapor present in the reactor when oxide is grown. This is a much slower and more expensive process but, the the quality of the films for graphene electronics is better. They will try to sell you wet oxide but don't buy it.

Before graphene deposition, alignment marks with a registry of  $100\mu\text{m}$  are fabricated on the sample using the Elionix e-beam writer. Also, cleaning the chip thoroughly is in order. The standard Marcus Lab recipe is to clean in acetone and isopropanol at room temperature for 5 minutes each. Then bake the chip at  $200^\circ\text{C}$  for 5 mins on a hot plate to remove any alcohol residue. Lastly, put the chip in a Samco UV/Ozone cleaner for 10 mins

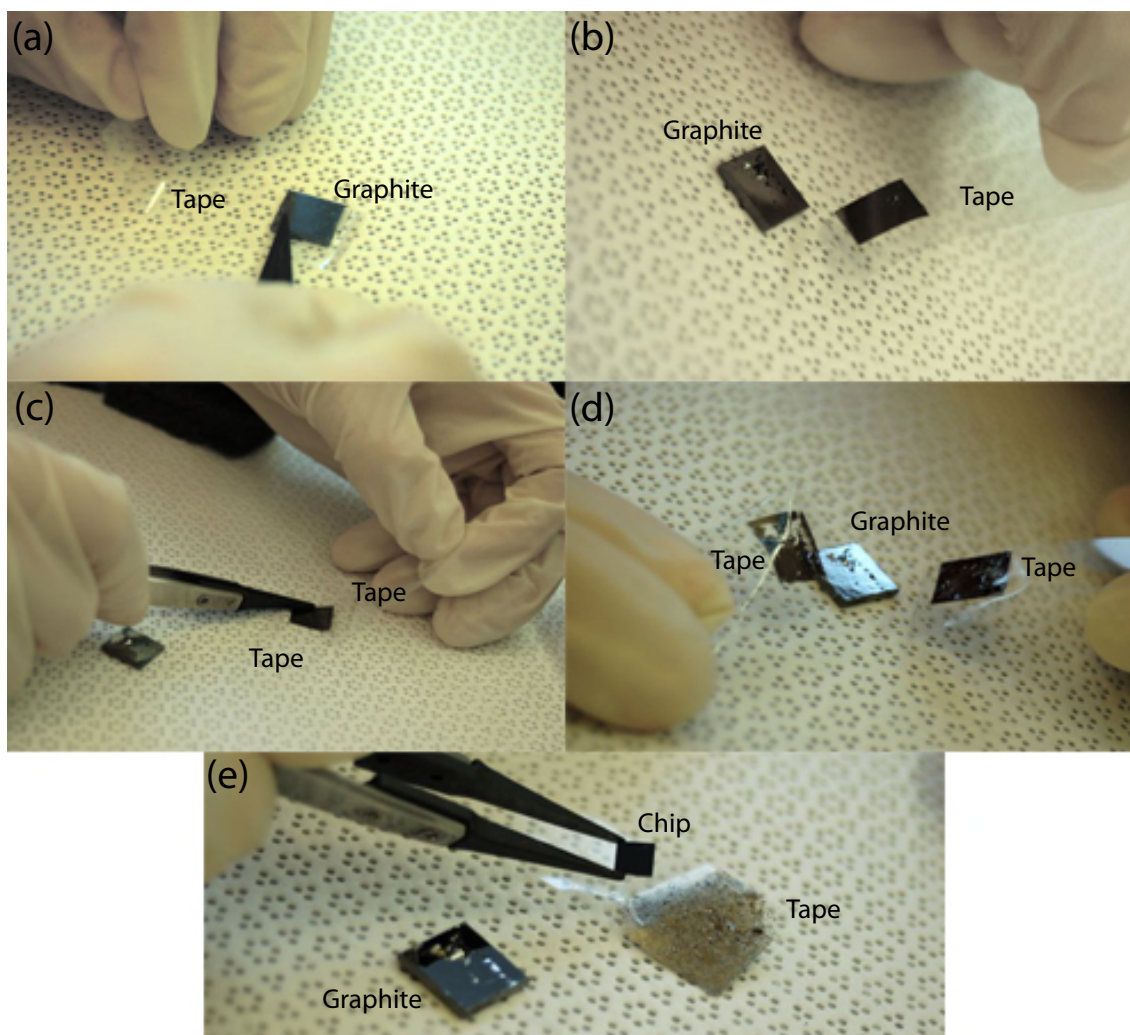


Figure A.2: (a) Cleave the graphite crystal by pressing the tape on the graphite surface and rubbing tweezers over the tape. (b) Peel the tape off the graphite, producing a thinner graphite square. (c) Take another piece of tape and press it on the tape covered with the graphite square, producing a tape-graphite-tape sandwich. (d) Peel apart the two pieces of tape. Take a fresh piece of tape and repeat the peel process until the tape surface looks like the tape in (e).

at room temperature. The flow rate of the  $O_2$  gas should be 1 SLM.

Place the chip, oxide side up, on a glass bowl that is roughly 1" thick [Fig. A.3(a)]. Take the tape with the light grey graphite on it, making sure no exposed areas of the tape touch the chip, and place it on the chip and rub the tweezers over it about 10 times [Fig. A.3(b)]. The resulting chip-tape-bowl configuration should look something like Fig. A.3(c). Place the bowl on a hot plate at  $180^\circ\text{C}$  for a total of 3 mins [Fig. A.4(a)]. At 1.5 mins, take

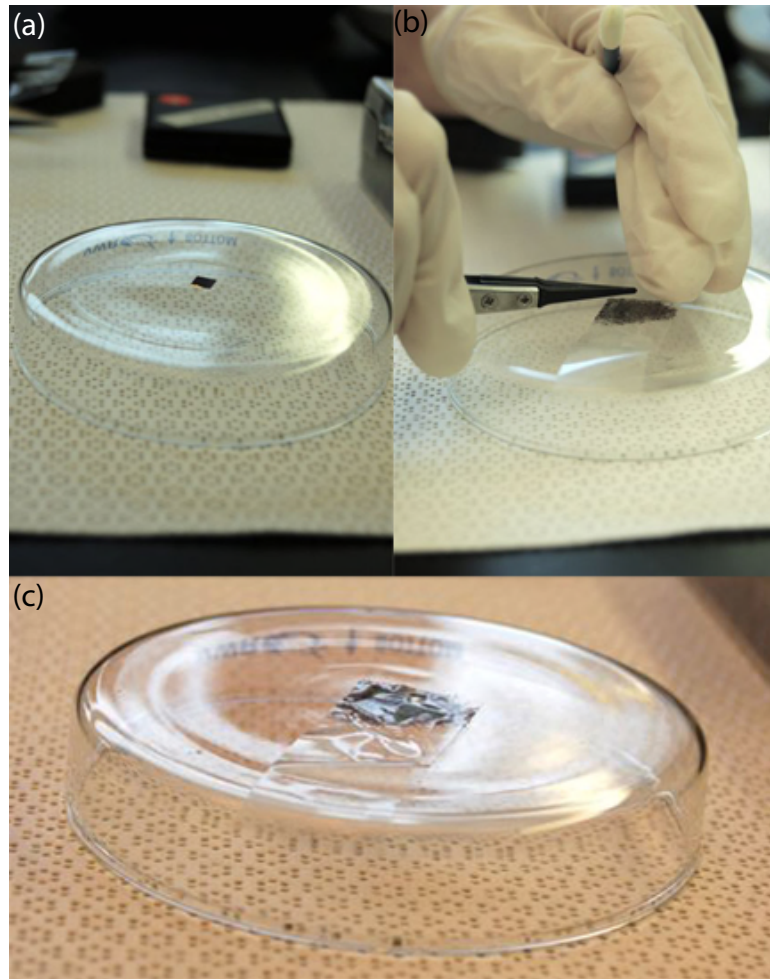


Figure A.3: (a) Place the on a glass bowl on the hot plate for

the bowl off the hot plate and tap it 5 times with a cleanroom swab [Fig. A.4(b)] and then place it back on the hot plate for the remaining 1.5 mins. A nice feature of this deposition method is that the tape is never rubber over the surface of chip, resulting in less transfer of tape residue to the surface. After the sample has cooled, remove the tape slowly and image the sample in the microscope.

Initial characterization on the graphene deposition is done via optical microscopy. Thin film interference is used to distinguish single layer graphene from bi- and multi-layer graphene sheets. There is an effervescent, light-purple glow that single layer graphene sheets will give off: so faint that it can be hard to see at first. An optical image of an area on the  $\text{SiO}_2$

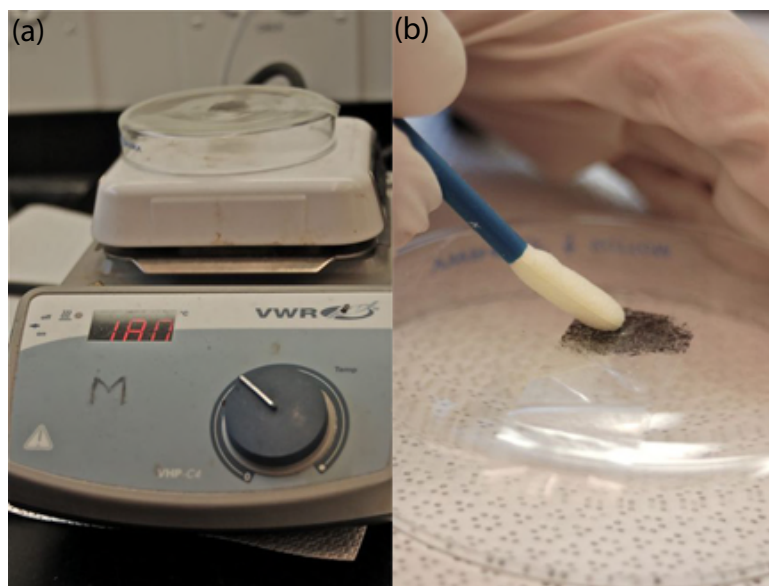


Figure A.4: (a) Place the chip on top of a glass bowl on a hot plate at 180°C for 1.5 mins. (b) Remove the plate and tap with a cleanroom swab 10 times. Place back on the hot plate for another 1.5 mins.

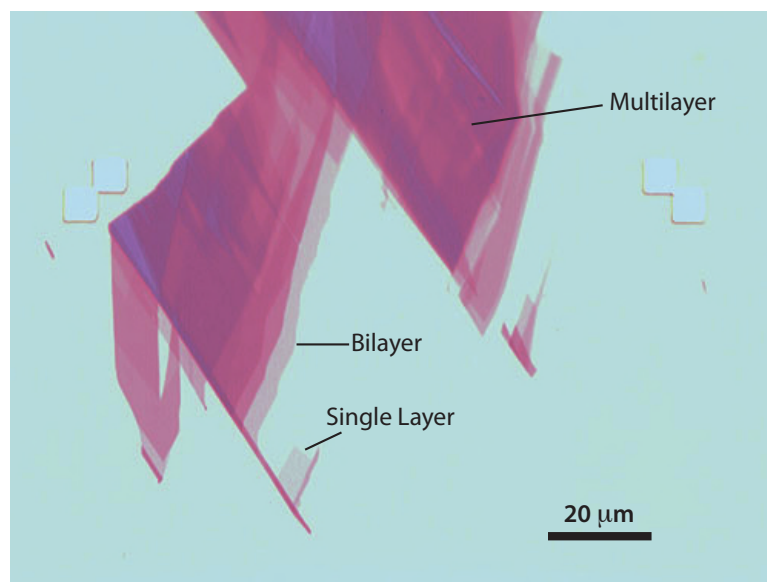


Figure A.5: An image of single, bi- and multi-layer graphene taken by an optical microscope.

that contains single, bi- and multi-layer graphene is shown in Fig. A.5.

## Appendix B

# Graphene $p$ - $n$ Junction Device Patent

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Microfabrication Of Carbon-Based Devices Such As Gate-Controlled Graphene  $p$ - $n$   
Junction Devices: U.S. Provisional Application No. 61/125,365 <sup>1</sup>

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<sup>1</sup>Prepared by Theresa Lober, T. A. Lober Patent Services

## **B.1 Cross-reference to related application**

[001] This application claims the benefit of U.S. Provisional Application No. 61/125,365, filed April 24, 2008, the entirety of which is hereby incorporated by reference.

## **B.2 Background of the invention**

[002] This invention relates to forms of carbon such as graphene and carbon nanotubes, and more particularly relates to microfabrication of carbon-based electronic devices.

[003] Graphene, a single-layer hexagonal lattice of carbon atoms, has recently emerged as a fascinating system for fundamental studies in condensed matter physics, as well as a candidate for novel sensors and post-silicon electronics. Carbon nanotubes (CNTs) and graphene are allotropes of carbon in which the carbon atomic orbitals rearrange to produce a solid in which electrical conduction is possible, as either a metallic or a semiconducting material. The differences in the electrical conduction properties of CNTs and graphene arise solely from the differences in their geometric structure. CNTs are solids in which the carbon atoms are arranged in a hexagonal lattice of a structure that is cylindrical and hollow. This structure is long in one direction, hundreds to thousands of nanometers, and short and confined in the other two directions, a few to tens of nanometers. This confinement is key to the CNT electronic properties. Depending on the diameter of the CNT, that is, how the CNT is rolled up, the electronic properties are either semiconducting or metallic. Exactly two-thirds of all CNT made are semiconducting while the remaining third are metallic, with the state-of-the-art CNT production technology unable to reliably make CNT of one type or the other.

[004] Although graphene is also a structure that is formed out of hexagonal lattices of carbon atoms, graphene is long in two directions and short in the other direction, resembling a sheet of chicken wire. This two-dimensional structure, in contrast to the CNT structure, is always metallic. The unusual band structure of single-layer graphene makes graphene a

zero-gap semiconductor with a linear, i.e., photon-like, energy-momentum relation near the points where valence and conduction bands meet. That is, a graphene sheet as-formed is always a metallic conductor.

[005] Graphene has the ability to carry electric current with either of the two electronic charge carrier types, electrons or holes. The entire modern bipolar electronics industry is based on devices that employ holes and electrons in device materials. In the semiconductor materials conventionally used for bipolar electronics, mainly silicon and germanium, the control of the particular charge carrier type in a device material is primarily achieved by a physical doping process such ion implantation, resulting in the creation of hole and electron regions in the implanted material. Such a doping method permanently fixes the location of the electron or hole regions in a semiconducting device. In addition, ion implantation fixes the charge carrier density, i.e., the number of charge carriers, either electron or holes, per square meter of the semiconducting material and device.

[006] It has been established that in startling contrast to this conventional charge carrier control by doping, control of electronic charge carrier type in graphene can be accomplished in a temporal fashion by the application of an electric field in the vicinity of a graphene region. Such an electric field can be produced by, e.g., a metal gate electrode provided near or at the surface of a graphene layer. A positive voltage on the gate electrode shifts the Fermi level of the graphene region under the electrode to produce a predominance of electron charge carriers in that region. A negative voltage on the gate electrode shifts the Fermi level of the graphene region under the electrode to produce a predominance of hole charge carriers in that region. A reversal of the voltage produces a corresponding reversal in charge carrier type. This phenomenon enables bipolar electronics in graphene to be completely reconfigurable, that is, a simple change in the gate electrode voltage allows for on-demand control of the carrier type and density that can be tuned to suit a particular graphene device application, and obviates the need for conventional physical and fixed doping, for instance via ion implantation.

### B.3 Summary of the invention

[007] The invention provides graphene configurations for producing robust and reproducible gate-controlled p-n junction devices having an arbitrary number of p-n junctions defined by regions having selected charge carrier types that are controlled temporally by one or more local gates. The summary language will directly paraphrase the claims and therefore will be added once we finalize the claims.

### B.4 Brief description of the drawings

[008] Figs. 1A-1B are schematic side views of two example graphene p-n junction devices provided by the invention and having a single top gate;

[009] Figs. 2A-2C are a schematic side representations of the device of Fig. 1B and two different charge carrier arrangements of that device, respectively, in accordance with the invention;

[010] Figs. 3A-3C are schematic side views of a further example graphene p-n junction device provided by the invention, having multiple top gates, in three different charge carrier arrangements in accordance with the invention;

[011] Figs. 4A-4B are schematic side views of a further example graphene p-n junction device provided by the invention, having multiple top gates and multiple p-n junctions, in two different charge carrier arrangements in accordance with the invention;

[012] Figs. 4C-4D are schematic side views of a further example graphene p-n junction device provided by the invention, having a single top gate and multiple p-n junctions, in two different charge carrier arrangements in accordance with the invention;

[013] Figs. 5A-5B are schematic top views of a p-n junction circuit arrangement, provided by the invention, in two different wiring configurations in accordance with the invention;

[014] Fig. 6 is a schematic representation of molecular species forming functionalization

and dielectric layers on a graphene layer in accordance with the invention;

[015] Fig. 7 is a schematic side view of an extrinsically undoped carbon nanotube including functionalization, dielectric, and gate material layers in accordance with the invention;

[016] Figs. 8A-8C are plots of differential conductance as a function of voltage of a carbon nanotube in a pristine state, after functionalization with HfO<sub>2</sub>, and after electron beam exposure in accordance with the invention, respectively,

[017] Figs. 9A-9D are plots of resistance and current as a function of voltage for an experimental graphene device having a configuration like that of the example device in Fig. 1A; and

[018] Figs. 10-10F are plots of conductance and magnetic field as a function of applied voltage for an experimental graphene device having a configuration like that of the example device in Fig. 1A.

## **B.5 Detailed description of the invention**

[019] Referring to Fig. 1A, there is shown a schematic cross-sectional view of an example graphene p-n junction device 10 provided by the invention. For clarity the dimensions of the device are not shown to scale. The device includes a layer of graphene 12 that in this example is configured with voltage biasing to produce one region of the layer biased as p-type and one region of the layer biased as n-type, in the manner described below. A global electrical connection is made to one side of the graphene layer, e.g., the backside surface, with a backgate electrode 14 that can be electrically insulated from the graphene 12 by, e.g., an insulating layer 16 if desired. Electrical device connection to the regions of the graphene to be biased n-type and p-type are made with device electrodes 18, 20, that directly contact the graphene. A local top gate 22 is provided directly above one of the device electrodes, in this example, over the left electrode 18. The top gate is electrically insulated from the graphene 12 and the device electrodes 18, 20 by a gate oxide layer 24. As explained in detail

below, the invention provides a functionalization layer 25 that is preferably included on the graphene to fully enable formation of the gate oxide layer without impacting the electrical properties of the graphene. Electrical connections 26, 28, 30, 32 are provided to the back electrode 14, device electrodes 18, 20, and local top gate 22, respectively.

[020] Fig. 1B is a schematic cross-sectional view of a further example graphene p-n junction device 33 provided by the invention that is equivalent to the first example in Fig. 1A. This device similarly includes a layer of graphene 12 and a backgate electrode 14 that can be electrically insulated from the graphene 12 by an insulating layer 16, and device electrodes 18, 20, that directly contact the graphene. A local top gate 35 is here provided above the right device electrode 20. The top gate is electrically insulated from the graphene 12 and the device electrodes 18, 20 by a gate oxide layer 24 and a functionalization layer 25, described in detail below. Electrical connections 26, 28, 30, 32 are provided to the back electrode 14, device electrodes 18, 20, and local top gate 22, respectively.

[021] With these graphene arrangements, the invention provides a temporally-controllable graphene p-n junction device in the manner shown in Figs. 2A-2C. In Fig. 2A the graphene p-n junction device 33 is represented highly schematically to focus on the voltage biasing for p-n junction device operation. With this arrangement, a backgate voltage, VBG, is applied to the backgate electrode 14. A device voltage, VD, is applied between the device electrodes 18, 20, for device operation. A top gate voltage, VTG, is applied to the local top gate 35. Depending on the relative top gate and backgate voltages, two distinct graphene regions 40, 42 are defined, one being n-type and the other being p-type, with a junction 45 at the border of the two regions.

[022] Referring to Fig. 2B, with the backgate voltage set as  $VBG \neq 0$ , and the top gate voltage set as  $VTG \neq 0 + (CTG/CBG)VBG$ , where CTG and CBG are the capacitances associated with the top gate and the backgate, respectively, the graphene region 42 under the top gate 35 is rendered n-type and the opposing region 40 is rendered p-type. The junction 45 between the n-type and p-type regions is at some mid-point between the device

electrodes 18, 20.

[023] This p-n junction arrangement can be reversed at will by applying the biasing of Fig. 2C. Here the backgate voltage is set as  $V_{BG} \neq 0$ , and the top gate voltage is set as  $V_{TG} \neq 0 + (CTG/CBG)V_{BG}$ , where CTG and CBG are the capacitances associated with the top gate and the backgate, respectively. With this biasing, the graphene region 42 under the top gate 35 is reversed to p-type and the opposing region 40 is reversed to n-type. The junction 45 between the n-type and p-type regions is again at some mid-point between the device electrodes 18, 20.

[024] With this example it is demonstrated that this graphene device of the invention enables temporal electronic control of the graphene layer to form a single p-type graphene region directly adjacent to a single n-type graphene region, with the carrier types of the two regions being reversible at will. Only one p-n junction is required and employed in this first example graphene device of the invention. A local top gate is disposed over one of the two graphene regions and therefore is disposed over the device electrode that is positioned at that region. This single-p-n junction device and the ability to control its doping profile temporally provide the foundation for a graphene-based bipolar technology that can surpass the current silicon-based bipolar technology in performance and application.

[025] In addition, beyond the myriad applications for graphene-based p-n junction devices in general, such a graphene p-n junction device is of great interest for studying many low-dimensional condensed matter physics phenomena. For instance, recent theory predicts that a local step in potential would allow solid-state realizations of relativistic, i.e., Klein, tunneling, and a surprising scattering effect known as Veselago lensing, comparable to scattering of electromagnetic waves in negative-index materials. The graphene p-n junction device of the invention thereby provides a platform for both device design as well as study of physical phenomena.

[026] The invention further provides graphene device and circuit arrangements in which more than one in a plurality of graphene regions are separately controlled by a corresponding

local top gate. As demonstrated below, these arrangements are temporally reconfigurable with any selected number of p-type and n-type graphene regions, each that can be individually addressed and with local top gate control, can be individually reversed in electronic charge carrier type.

[027] Referring to Figs. 3A-3B, this configuration is schematically represented for a first example of a single p-n junction graphene device 50. The graphene device here includes a graphene layer 12 having a first region 40 and a second region 42 that are defined with charge carrier types based on the applied top gate voltages as described below. For clarity, a global backgate electrode 14 is here shown biased at ground. Device electrodes 18, 20 are biased with a selected device voltage,  $V_D$ , applied between the electrodes.

[028] Local top gate electrodes 35, 37 are provided over the graphene, separated from the graphene by a gate insulator 24 and a functionalization layer that is not here shown for clarity. With the first top gate electrode 35 biased with an appropriate positive voltage 66 and the second top gate electrode 37 biased with an appropriate negative voltage 68, an n-type graphene region 40 is formed under the first top gate electrode 35 and a p-type graphene region 42 is formed under the second top gate electrode 37. The required top gate bias voltages are to be understood to include a consideration of device capacitances, as in Figs. 2B-2C.

[029] As shown in Fig. 3B, the top gate voltages can be each controlled to reverse the polarity of the p-n junction configuration of Fig. 3A. With the first top gate electrode 35 biased with an appropriate negative voltage 66 and the second top gate electrode 37 biased with an appropriate positive voltage 68, the graphene region 40 under the first top gate electrode 35 is reversed to p-type and the graphene region 42 under the second top gate electrode 37 is reversed to n-type; the polarity of the p-n junction is thusly reversed. This localized control can be extended, as shown in Fig. 3C, with both the first and second top gate electrodes 35, 37 biased with appropriate positive voltages 66, 68, whereby the graphene region 40 under the first top gate electrode 35 is reversed back to n-type, as in

Fig. 3A, and as in the adjacent n-type graphene region 42. This configuration eliminates the p-n junction from the device

[030] This example demonstrates that the graphene layer can be electrically controlled locally with top gates to form two adjacent graphene regions of opposite conductivity type, producing a p-n junction at the interface of the regions, then can be controlled to reverse the polarity of the p-n junction, and further can be controlled to set the regions to be of the same conductivity type, thereby eliminating the p-n junction entirely. The local top gating arrangement provided by the invention enables this control; the charge carrier type of each region is reversed simply by reversal of a gate electrode voltage from  $+V$  to  $V$  or from  $V$  to  $+V$ . While this procedure is here demonstrated for a single graphene p-n junction device, it is applicable to all graphene p-n junction device and circuit arrangements provided by the invention.

[031] For example, referring to Figs. 4A-4B, this paradigm is extended to a two-junction graphene device 70. The graphene device here includes a graphene layer 12 having a first region 40, a second region 42, and a third region 43 each of which are formed with a selected carrier type by application of a selected voltage applied to a top gate electrode disposed atop that region. For clarity, a global backgate electrode 14 is here shown biased at ground. Device electrodes 18, 20 are biased with a selected device voltage,  $V_D$ , applied between those electrodes.

[032] Local top gate electrodes 35, 37, 39 are provided over the graphene 12, separated from the graphene by a gate insulator 24 and a functionalization layer not here shown for clarity. With the first and second top gate electrodes 35, 37 biased with an appropriate positive voltage 66, 68 and the third top gate electrode 39 biased with an appropriate negative voltage 69, n-type graphene regions 40, 42 are formed under the first and second top gate electrodes 35, 37, and a p-type graphene region 43 is formed under the third top gate electrode 39, producing an n-p-n arrangement for, e.g., a transistor device. The applied top gate bias voltages are to be understood to include a consideration of device

capacitances, as in Figs. 2B-2C.

[033] Note in this configuration that no device electrode is disposed under the third top gate electrode 39. The invention does not require that each and every top gate be paired with a corresponding device electrode. For the graphene device 70 of Fig. 4A, if there is no need to make electrical contact to the third graphene region 43, then no device electrode need be provided at that region. But with local top gating of all three regions, the polarity of the two p-n junctions 51, 53, of the device can be reversed, and one or both of the p-n junctions can be eliminated.

[034] Referring to Fig. 4B, such control of the p-n junctions can reconfigure the transistor device 70 of Fig. 4A to a diode or other single-junction device 72 as in Fig. 4B. Here the first top gate electrode 35 is biased with an appropriate positive voltage 66 and second and third top gate electrodes 37, 39, are biased with appropriate negative voltage 68, 69. With this top gate biasing, an n-type graphene region 40 is formed under the first top gate electrode 35 and two p-type graphene regions 42, 43 are formed under the second and third top gate electrodes 37, 39, resulting in a single p-n junction 45 under the three top gates that can be employed in a diode or other single-junction device.

[035] Referring to Fig. 4C, in a further embodiment of the invention, a two-junction graphene device 74 is produced with a graphene layer 12 that is here configured with three device electrodes 18, 20, 23, adjacent to the graphene layer, for applying device voltage biases 60, 62, 63, between the three device electrodes. The third device electrode 23 is contacted at an edge of the device; the representation of this contact arrangement is schematic only to provide clarity of the device regions. In the configuration of Fig. 4C, a sole local top gate 39 is provided and is located over the third device electrode 23. This top gate 39 is biased with an appropriate positive voltage 69 that forms an n-type graphene region 43 under the top gate 39 and two p-type graphene regions 40, 42, adjacent to each side of the n-type region 43. Only one top gate is here employed to form the three distinct graphene regions, and the three device electrodes provided for making electrical contact to

each of the three graphene regions enable complete device control, with one of the three device electrodes provided under the top gate. [036] Referring also to Fig. 4D, the polarity of this two-junction graphene device 74 can be reversed by simply reversing the polarity of the top gate bias to an appropriate negative voltage 69. The two p-type regions are then reversed to n-type regions 40, 42, and the n-type region is reversed to a p-type region 43. As stated just above, each of the three regions is individually contacted by device electrodes 18, 20, 23, that enable full control of the device before, during, and after the polarity reversal.

[037] This control of p-n junction polarity and the formation and elimination of p-n junctions can be extended to any arbitrary number of junctions and to both device and circuit arrangements. For example, referring now to Fig. 5A, there is schematically shown an example four-terminal graphene circuit 80 in accordance with the invention. To clarify this arrangement, the circuit is represented in a top-down view with the top gates not shown. Each of the three identified p-type graphene regions 82, 84, 86, and each of the three identified n-type regions 88, 90, 92, have a top gate that is physically located over the region and is biased with an appropriate polarity voltage,  $VTG,p$ , and  $VTG,n$ , in the manner described above to produce the indicated charge carrier type in that region. Each of the regions further is connected to one of four device contacts 94, 96, 98, 100. An arrangement of p-type and n-type regions such as this can only be achieved with the local top gating provided by the invention.

[038] This graphene circuit 80 enables reconfigurable wiring by exploiting so-called snake states that exist at a p-n interface. Specifically, enhanced electrical conduction at each p-n interface effectively forms a one-dimensional wire that is physically located at the junction between each p-type and n-type region. With this condition set, the arrangement of the circuit 80 in Fig. 5A, results in an enhancement of conductance between the first and third device electrodes 94, 98, thereby forming a path of enhanced conduction, or a one-dimensional wire 102, between these electrodes 94, 98 solely through control of the top gate voltages to set the p-type and n-type regions as shown.

[039] Referring also to Fig. 5B, the circuit therefore can be rewired to provide a different selected wiring connection 105, e.g., to connect the first and fourth device electrodes 94, 100, by switching the polarity of the top gate over one region 92, reversing the charge carrier type of that region 92 from n-type to p-type. Here the circuit connection of the first arrangement 80 is eliminated and a new path of enhanced conduction 104 is formed, between the first and fourth device electrodes 94, 100. Any number of p-n junction circuit configurations like these can be controlled to thusly form temporal wiring connections between selected device electrodes.

[040] These examples demonstrate that in accordance with the invention, each designated region of graphene to be controlled as a specific charge carrier type can be individually controlled with a corresponding top gate as-desired, but need not be; in either case, adjacent n-type and p-type conducting regions of graphene can be controlled to coexist by individual biasing of at least one of the adjacent regions. As a result, an arbitrary number of p-n junctions, including a single p-n junction, can be produced within a single graphene layer in accordance with the invention. Each distinct charge carrier region produced in the graphene layer with a corresponding local top gate can also be individually contacted under the top gate for device biasing and operational device control.

[041] The invention provides specific processes for fabricating the graphene devices, circuits, and systems of the invention. It is recognized in accordance with the invention that for any graphene-based technology to succeed, the graphene behavior must meet the demands of modern electronics including stability and reproducibility. In general, stable electronics require that the properties of a device remain static over time. But graphene is known to interact with water in even only relatively humid environments, causing electronic charge hole doping of an exposed graphene region. The resulting hole charge carrier concentration in the graphene is related to the amount of water in the environment and, therefore, changes as the ambient humidity changes. In pristine graphene, i.e., graphene with no external doping, there is no excess electron or hole charge carrier concentration. The excess

charge carrier concentration in graphene caused by extrinsic doping due to environmental conditions gives rise to reduced mobility in a graphene device, which places limits on the speed at which the device can operate. Also, for a given electric field range, extrinsic doping limits the carrier density and, if the doping is strong enough, the carrier type that can be utilized in a graphene device. The level of doping in a graphene device can be ascertained by sweeping the voltage,  $V$ , on a gate electrode while measuring the resistance of the device. If the peak in resistance, or corresponding dip in conductance, is at or very near the point of zero voltage bias, the device is undoped. If the peak in resistance occurs very far away from the zero voltage bias, the device is doped.

[042] It is recognized in accordance with the invention that permanent prevention of external doping of graphene in a graphene device is particularly preferred to preserve graphene device performance characteristics. To prohibit such external doping, in accordance with the invention a graphene layer to be employed in a device or circuit is protected to prevent environmental changes to the device in which the graphene is employed. The form of this graphene protection can be implemented as a function of a desired device configuration. For example, where one or more local top gates are employed to control regions of a graphene sheet, the gates are separated from the graphene sheet by a gate oxide layer. The gate oxide layer can operate to shield the graphene from the environment if, in accordance with the invention, the oxide layer is a blanket layer, not a regional or sectioned area, and the blanket layer covers the entire graphene surface, not just the regions directly beneath the gate electrodes, to protect the entire graphene surface from the environment and thereby prevent unintended doping of the graphene surface. Thus, it is preferred to blanket-passivate a graphene layer or device to limit the transient nature of the device properties that would be produced in a humid environment. Local oxide formation, rather than blanket formation, would not fully passivate a graphene device; leaving exposed graphene surface areas that can absorb molecules, resulting in reduced device functionality. In addition, local oxide formation requires serial processing, in turn requiring long processing times for wafer-scale

device fabrication.

[043] Because graphene is very reactive with even its immediate environment, the choice of a blanket gate oxide material is particularly important. Many physical deposition methods result in amorphous oxides that can dope a graphene layer such that the layer exhibits the aforementioned degraded qualities. It is further discovered in accordance with the invention that the surface of graphene is chemically inert to many oxide deposition methods like Atomic Layer Deposition (ALD), preventing all oxide growth by that technique.

[044] In accordance with the invention, to enable the formation of a selected oxide blanket layer on a graphene sheet, a noncovalent functionalization layer is first provided on the surface of the graphene layer in a manner that provides functional species that can react with deposition precursors to form a blanket coating of a selected oxide. Specifically, functionalization layer is provided to impart a catalytically-suitable surface for growth of oxides, such as high-k dielectrics, via vapor processes such as ALD. The functionalization layer also passivates the graphene surface such that an oxide formed on the functionalization layer does not impact the electronic properties of the graphene.

[045] The functionalization layer is compatible with a wide range of oxide type and deposition methods. For ALD, the functionalization layer allows for the deposition of, e.g.,  $\text{Al}_2\text{O}_3$ ,  $\text{HfO}_2$ , and  $\text{ZnO}$ , all of which are commonly employed as high-k dielectric layers. The functionalization layer can also be employed for carrying out physical vapor deposition and chemical vapor deposition processes to form blanket oxide layers of, e.g., silicon dioxide, titanium oxide, or ferroelectric materials like lead zirconate titanate (PZT). With the functionalization layer in place on the graphene prior to the dielectric formation, the dielectric does not extrinsically dope the graphene or otherwise impact the electronic properties of the graphene layer.

[046] The functionalization layer and blanket oxide layer are formed in accordance with the invention on a graphene layer once such is provided in place on a selected substrate or other structure. It is recognized that many techniques exist and are being developed to

produce graphene sheets. The invention is not limited to any particular graphene production process or resulting graphene configuration. In one example process to produce a piece of graphene, a thin piece of graphite is first extracted from, e.g., a bulk piece of highly oriented pyrolytic graphite, such as SPI-1 grade graphite, from SPI Supplies, Structure Probe, Inc., [www.2spi.com](http://www.2spi.com). The extraction is carried out using, e.g., an adhesive tape, such as 3M Mask PlusII - Water Soluble Wave Solder Tape, from 3M, [www.3m.com](http://www.3m.com), by applying the tape to the graphite. The graphite region that is extracted onto the tape is thinned by repeated exfoliation of the region with additional tape.

[047] Prior to a final exfoliation step, a selected substrate is provided, onto which the graphene is to be arranged. In one example, where a graphene device with a backgate electrode is desired, a heavily doped substrate, such as an n++ Si substrate, can be employed as the support substrate and as the backgate electrode. Where the backgate electrode is to be electrically isolated from the graphene, as in the configurations of Figs. 1A-1B, a layer of oxide is provided on the top surface of the Si substrate. In one example, a layer of SiO<sub>2</sub>, e.g., a 300 nm-thick, thermally grown layer of SiO<sub>2</sub>, is formed on the silicon substrate and then is cleaned in acetone and isopropyl alcohol (IPA).

[048] Tape from the final graphene exfoliation is pressed against the oxide layer on the substrate and rubbed gently, e.g., with the back of a tweezers, for some reasonable time, e.g., 10 seconds. The structure is then immersed in water, e.g., at 60C, to dissolve the tape from the graphene, and the substrate is preferably again cleaned in acetone and IPA to remove any tape residue left on the graphene and substrate surface. The structure can then be viewed under an optical microscope to identify potential regions of graphene using the well-established condition in which a single layer of graphene causes a characteristic color shift that arises from thin-film interference and that is distinct from two, three or more such layers.

[049] Other graphene formation and arrangement techniques can be employed and the invention contemplates the future development of graphene formation processes that are

more efficient and effective than those currently employed. The invention is not limited to current graphene production processes and is applicable to a graphene layer produced by any method.

[050] With a graphene sheet, layer, or region in place on a selected platform, such as a microelectronic substrate, a graphene device, circuit, or other system in accordance with the invention can be produced with the functionalization and blanket oxide layers described above. To demonstrate the graphene microfabrication processes of the invention, one example process for producing the devices of Figs. 1A-1B is described below, but the invention is not limited to such. It will be readily apparent that this process is applicable to all of the graphene devices and circuits described above and indeed, to any graphene device in which the layer of graphene is to be electrically connected for biasing and for device or circuit operation.

[051] Referring then back to Fig. 1A, in this example fabrication sequence, with a graphene layer 12 provided on an oxide layer 16 of a silicon substrate 14 as described above, electrically conducting device electrodes 18, 20 are formed directly on the graphene. It is preferred that the device electrodes be provided directly on the graphene, not separated from the graphene by functionalization or oxide layers. In one example process to form the device electrodes, a resist, e.g., PMMA, is spin-coated onto the graphene and lithography, e.g., electron-beam lithography, is carried out to define in the resist specified locations of graphene device electrodes. The electrode material is then deposited by, e.g., a physical deposition process such as thermal evaporation. In one example, the electrode material is provided as a 40 nm-thick layer of gold layered on top of a 5 nm-thick layer of titanium. Titanium can be preferred to ensure good electrical contact to the graphene and an upper gold layer can be preferred to prevent the titanium from oxidizing and to provide good electrode conductivity. Then using conventional lift-off techniques the resist is removed and the device electrodes 18, 20 are formed on the graphene. With the device electrodes in place, a blanket top gate oxide layer 24 in Fig. 1A is to be provided over the electrodes and

the graphene to operate both as a gate oxide layer and as a layer of protection against the environment.

[052] As explained above, in accordance with the invention, prior to such oxide layer formation, a functionalization layer is first formed over the graphene in a blanket fashion, thereby also covering the device electrodes. The functionalization layer provides chemically functional groups at the graphene surface to enable deposition of an oxide layer on the graphene surface. Preferably the functionalization layer only non-covalently bonds with the graphene surface while providing the chemically functional groups for enabling deposition of a material on the graphene surface.

[053] In one functionalization layer formation process in accordance with the invention, the structure is cleaned, e.g., with acetone and IPA, and then inserted into an ALD reaction chamber, e.g., a Cambridge Nano Tech Savannah Atomic Layer Deposition Tool, Cambridge Nano Tech, Inc., [www.cambridgenanotech.com](http://www.cambridgenanotech.com). An ALD process is then carried out to form a functionalization layer that is based on precursors for producing an upper oxide layer of  $\text{Al}_2\text{O}_3$ .

[054] In one example functionalization/passivation process, nitrogen dioxide gas ( $\text{NO}_2$ ) and trimethylaluminum (TMA) vapor are employed to form a functionalization layer. In this example process, the chamber is pumped down to a pressure of, e.g., about 0.3 torr. Next, the functionalization layer is deposited at room temperature with a number of cycles, e.g., about 50 cycles, of the following sequence. A 100 torr dose of  $\text{NO}_2$  is first introduced into the chamber for, e.g., about 0.5 seconds and then pumped out. Following a 7 second purge under continuous flow of 20 sccm of nitrogen gas ( $\text{N}_2$ ), a 1 torr dose of trimethylaluminum TMA vapor is pulsed into the chamber. The chamber is then purged for 2 minutes before beginning the next cycle.

[055] With this functionalization layer in place, a thin layer is applied to prevent the functionalization layer from desorbing. Then the gate oxide is formed on the stabilized functionalization layer. For many applications, it can be preferred to form the gate oxide

layer by the same process as the functionalization layer, e.g., by ALD. In one example process of such, immediately after the functionalization layer cycles, e.g., 50 ALD cycles of the process just above, a thin layer of  $\text{Al}_2\text{O}_3$  is formed by ALD on the functionalization layer to prevent desorption. This thin layer is grown by, e.g., 5 ALD cycles at room temperature of, e.g., a 1 torr pulse of  $\text{H}_2\text{O}$  vapor followed by a 1 torr pulse of TMA vapor, under continuous flow of  $\text{N}_2$ , with 5 second-intervals provided between pulses.

[056] A top gate oxide layer of, e.g.,  $\text{Al}_2\text{O}_3$ , in this example, is then grown on the stabilized functionalization layer. In one example process, the ALD temperature is raised to about 225C and a selected number of cycles, e.g., 300 cycles, of a 1 torr pulse of  $\text{H}_2\text{O}$  vapor followed by a 1 torr pulse of TMA vapor, under continuous flow of  $\text{N}_2$ , with 5 second-intervals provided between pulses are carried out. In this process, each  $\text{H}_2\text{O}$ -TMA cycle adds about 1 Angstrom of  $\text{Al}_2\text{O}_3$  to the layer. A 300-cycle process thereby produces a total oxide thickness of about 30 nanometers. Given the precision of the ALD formation process, a wide range of oxide thicknesses can be obtained as-desired. Oxide layers as thin as about 10 nm and as thick as desired, e.g., 100 nm or more, given that there is no upper limit on the oxide thickness, can be provided with this formation method. The method is also quite flexible in temperature; ALD growth can be carried out at temperatures as low as about 80C and as high as about 225C.

[057] Referring to Fig. 6, with this oxide formation complete, a layer of  $\text{Al}_2\text{O}_3$  24 is provided on a functionalization layer 25 that blanket-coats the graphene 12 and any graphene region device electrodes, which are not shown here for clarity. The functionalization layer forms a non-interacting layer between the graphene and the top gate oxide layer, thereby preserving the electronic properties of the underlying graphene, and provides a surface that is catalytically suitable for the formation on the graphene of a gate oxide layer by a selected process such as ALD. Additional details and alternatives for functionalization layer formation are provided in U.S. Patent Application Publication US2008-0296537, entitled, Gas-phase functionalization of carbon nanotubes, published December 4, 2008, the entirety

of which is hereby incorporated by reference.

[058] The invention is not limited to a particular functionalization layer formation process or functionalization layer material and can be conducted with any suitable set of precursors that non-covalently bind with the graphene surface to form a catalytically-active surface on which can be formed an oxide layer. For many applications, it can be preferred to employ as a functionalization layer precursor one of the precursors that is to be employed in formation of the subsequently formed oxide layer. Where a high-k dielectric is to be employed as the oxide layer, e.g., Hafnium Oxide (HfO<sub>2</sub>) or zinc oxide (ZnO), or it can be preferred to provide a functionalization layer that is based on the selected oxide layer.

[059] For example, given a graphene device process in which HfO<sub>2</sub> is to be employed as a top gate oxide material, a functionalization layer in accordance with the invention can employ an HfO<sub>2</sub> precursor in the formation of the PFL. In one example process provided by the invention for producing such, a graphene layer, provided on a substrate and having device electrodes formed on the graphene, if desired, in the manner described above, is cleaned, e.g., with acetone and IPA, and the substrate is inserted into an ALD reaction chamber. The chamber is pumped down to a suitable pressure, e.g., about 0.3 torr. A number of ALD cycles, e.g., 50 cycles, are then carried out at, e.g., room temperature, to form a functionalization layer by the following process. A 100 torr dose of NO<sub>2</sub> gas is first introduced into the chamber for about 0.5 seconds and then pumped out. Following a 10 second purge under continuous flow of 20 sccm of N<sub>2</sub>, a 1 torr dose of tetrakis(dimethylamido)hafnium(IV) (TDH) vapor is pulsed into the chamber. The chamber is then purged for, e.g., about 5 minutes before beginning the next cycle. The resulting functionalization layer is then capped, in the manner described above, to prevent desorption, by performing 5 cycles of 1-torr pulses of H<sub>2</sub>O and 1.5 torr pulses of TDH, deposited at room temperature.

[060] With this step, a stable functionalization layer is formed on the graphene layer and is ready for formation of a top gate oxide layer. Here, e.g., a layer of HfO<sub>2</sub> can be directly formed on the functionalization layer in the ALD chamber with the TDH precursor. The

layer of HfO<sub>2</sub> can be deposited with a selected number of cycles each employing a 1 torr pulse of H<sub>2</sub>O vapor and a 1.5 torr pulse of TDH vapor, under continuous flow of N<sub>2</sub> and with 20 seconds intervals between the pulses. This cyclic HfO<sub>2</sub> deposition can be performed at a variety of temperatures, e.g., between about 80C and about 300C. The invention contemplates other functionalization layers and other oxide layers.

[061] It has been discovered in accordance with the invention that even with a functionalization layer provided on a graphene surface, some dielectric layers cause extrinsic doping of the graphene. This is not in general true; for example, an Al<sub>2</sub>O<sub>3</sub> gate oxide layer formed on a TMA-based functionalization layer does not extrinsically dope or otherwise impact the electronic properties of an underlying graphene layer. But other oxide layers, for example, HfO<sub>2</sub>, can extrinsically dope the underlying graphene layer, even in the presence of the functionalization layer, and further can reduce the electronic charge carrier mobility of the underlying graphene.

[062] In accordance with the invention, after a functionalization layer is formed or after a top gate oxide layer is formed on a functionalized graphene device or circuit layer, it is preferred to conduct a current-voltage measurement of the device or circuit to determine if the functionalization layer or the oxide layer has impacted the electronic properties of the graphene. If the graphene does not exhibit the undoped current-voltage relation that is characteristic of pristine graphene, then a compensation process is carried out in accordance with the invention to restore the undoped characteristic of the graphene.

[063] In one example compensation process provided by the invention, an energetic beam, e.g., an electron beam, is rastered across the surface of the oxide layer. In one example, a high-energy electron beam of electrons at a voltage of, e.g., about 30 keV, is rastered very quickly over the oxide surface, to expose the oxide to the electron beam for, e.g., about 10 ms/m<sup>2</sup>. This process can be carried out a number of cycles, and the beam voltage and raster rate can be adjusted in a manner suitable for a given application, such that electrons penetrate a selected depth through the oxide and functionalization layers.

[064] It is understood in accordance with the invention that the electron beam exposure of a functionalization layer and/or oxide layer can passivate molecular dangling bonds that can exist in the oxide and underlying functionalization layer. The resulting passivated oxide and functionalization layers then do not need to accept or donate electrons from the graphene, rendering the graphene charge-neutral and preserving the unique electronic properties of the graphene. With this understanding, it can be preferred in accordance with the invention to evaluate the charge state of a graphene layer after top gate oxide formation to determine if this charge compensation process of the invention is warranted.

[065] Now referring back to Fig. 1A, with an oxide layer 25 in place on a functionalization layer 25 over the graphene 12, one or more top gates 22 are formed on the oxide layer surface. It is to be recognized that any suitable gate dielectric material can be employed and the oxide layers described above are examples of such, but are not limiting.

[066] The top gates can be formed in the manner of the device electrodes, with metal evaporation and lift-off patterning processes. For example, a resist such as PMMA can be spin-coated over the oxide surface and patterned by, e.g., electron-beam lithography to define regions for location of top gates. The top gate electrodes are then deposited by, e.g., thermally evaporating a 5 nm-thick layer of titanium and 40 nm-thick layer of gold in the manner described above, with a lift-off process employed to remove the metals and the resist in formation of one or more top gates. With the top gate formation complete, a locally-gated graphene p-n junction device in accordance with the invention is produced.

[067] This graphene device production process can be extended to the production of electrically-gated carbon nanotube devices, or indeed, production of any carbon-based material device, whether or not including a gate electrode, in accordance with the invention. Referring to Fig. 7, there is provided by the invention such an example, here a gated carbon nanotube device 150. The carbon nanotube device includes a carbon nanotube 152 having a coaxial functionalization layer 154 on its cylindrical wall surface. A coaxial gate oxide layer 156 is provided over the functionalization layer, and a coaxial gate electrode 158 is

provided at a selected point along the cylindrical wall surface of the carbon nanotube.

[068] The functionalization layer 154 is formed on the nanotube in the manner described above, preferably with an ALD process that employs a precursor that is also used for forming the gate oxide layer 156, e.g.,  $\text{Al}_2\text{O}_3$  or  $\text{HfO}_2$ , or other selected gate oxide material. After the gate oxide layer is formed, the carbon nanotube is electrically contacted at its ends to determine if the nanotube has been extrinsically doped by the functionalization and/or oxide layers. If so, then the electron beam rastering process described above is carried out to compensate for the extrinsic doping and to render the nanotube with the characteristics of that of a pristine carbon nanotube.

[069] After such electron beam rastering of the nanotube, a gate electrode can be formed on the nanotube, either at a specific point or coaxially around the circumference of the nanotube. The electron beam rastering of the gate oxide enables the production of a gated carbon nanotube that is not extrinsically doped by the environment or the layers deposited on the nanotube. This demonstrates that the functionalization and oxide layer formation processes of the invention, in conjunction with the electron beam compensation process of the invention, can be applied to carbon-based structures in general, and is not limited to graphene

## B.6 Example I

[070] A semiconducting carbon nanotube was synthesized by methane CVD and was configured for initial conductance characterization in a pristine state. A source-drain dc transport measurement was made by contacting ends of the nanotube. Fig. 8A is a plot of differential conductance,  $g$ , as a function of backgate voltage,  $V$ , for the pristine nanotube.

[071] The carbon nanotube was then processed to form a functionalization layer and an oxide layer on the full circumference and length of the cylindrical sidewall of the nanotube. The nanotube was inserted into an ALD reaction chamber and the chamber was

pumped down to a pressure of 0.3 torr. 5 ALD cycles were then conducted at room temperature to form a functionalization layer by the following process. A 100 torr dose of NO<sub>2</sub> gas was first introduced into the chamber for 0.5 seconds and then pumped out. Following a 10 second purge under continuous flow of 20 sccm of N<sub>2</sub>, a 1 torr dose of tetrakis(dimethylamido)hafnium(IV) (TDH) vapor was pulsed into the chamber. The chamber was then purged for, e.g., about 5 minutes before beginning the next cycle.

[072] The resulting functionalization layer was then capped and a layer of HfO<sub>2</sub> formed by 5 ALD cycles employing a 1 torr pulse of H<sub>2</sub>O vapor and a 1.5 torr pulse of TDH vapor, under continuous flow of N<sub>2</sub> and with 20 seconds intervals between the pulses at room temperature. With the oxide and functionalization layers formed, a source-drain dc transport measurement was again made at room temperature as a function of gate voltage. Fig. 8B is a plot of differential conductance,  $g$ , as a function of voltage,  $V$ , for the structure. As shown by the plot, the neutrality point for the device was dramatically shifted away from the 0-volt point by the functionalization and oxide layers.

[073] The HfO<sub>2</sub>-coated nanotube was then exposed to rastering of an electron beam across the oxide surface to impose a dose of 100  $\mu\text{C}/\text{cm}^2$  on the structure.

[074] Fig. 8C is a plot of differential conductance,  $g$ , as a function of voltage,  $V$ , for the structure after the electron beam processing. The electron beam processing was found to clearly compensate for the extrinsic doping of the carbon nanotube to set the neutrality point back to around 0 V.

## B.7 Example II

[075] A graphene device having the configuration of Fig. 1A was microfabricated in accordance with the invention. A 300 nm-thick layer of SiO<sub>2</sub> was thermally grown on a degenerately doped Si wafer. Graphene was exfoliated with a taping technique and applied to the oxide surface, and was identified by thin-film interference. Two device electrodes

were formed by electron beam lithography and lift off with layers of titanium and gold, of 5 nm and 40 nm in thickness, respectively. A functionalization layer was then formed by the ALD process described above, employing 50 pulsed cycles of NO<sub>2</sub> and TMA at room temperature, in the manner given above. The functionalization layer was then stabilized by a 5-cycle ALD process of H<sub>2</sub>O and TMA at room temperature, also in the manner given above. An oxide layer of Al<sub>2</sub>O<sub>3</sub> was then formed over the stabilized functionalization layer by 300 ALD cycles of pulsed H<sub>2</sub>O/TMA, at a temperature of about 225°C, yielding an oxide thickness of about 30 nm. To complete the device, a local top gate was formed as in Fig. 1A by electron beam lithography and lift off with layers of titanium and gold, of 5 nm and 40 nm in thickness, respectively. The top gate was located over one of the device electrodes just as in Fig. 1A.

[076] The completed device was cooled in a <sup>3</sup>He refrigerator and characterized at temperatures of 250 mK and 4.2 K. Differential resistance,  $R=dV/dI$ , where  $I$  is the current and  $V$  the source-drain voltage, was measured by standard lock-in techniques with a current bias of 1 nA rms at 95 Hz for  $T=250$  mK (4.2K). The voltage across the two device electrodes contacting the graphene layer, was measured in a four-wire configuration, eliminating series resistance of the cryostat lines, but not contact resistance. Contact resistance was evidently low ( $< 1$  k), and no background was subtracted from the data.

[077] A measurement of the differential resistance,  $R$ , as a function of back-gate voltage, VBG, and top-gate voltage, VTG, at magnetic field  $B=0$ , is provided in the plot of Fig. 9A. This plot demonstrated independent control of carrier type and density in the two graphene regions. This two-dimensional plot reveals a skewed, cross-like pattern that separates the space of top gate and backgate voltages into four quadrants of well-defined carrier type in the two regions of the graphene. The horizontal (diagonal) ridge corresponds to charge-neutrality, i.e., the Dirac point, in region 1. The slope of the charge-neutral line in region 2, along with the known distances to the top gate and back gate, gives a dielectric constant  $\epsilon \approx 6$  for the functionalized Al<sub>2</sub>O<sub>3</sub>. The center of the cross at (VTG, VBG) is (-0.2 V, -2.5

V) corresponds to charge neutrality across the entire graphene layer. Its proximity to the origin of gate voltages demonstrates that the functionalized oxide did not chemically dope the graphene significantly.

[078] Data for slices through this 2-D conductance plot at a fixed top gate voltage, VTG, are shown in the plot of Fig. 9C. The slice at VTG=0 shows a single peak commonly observed in devices with only a global back gate. Using a Drude model away from the charge-neutrality region, mobility is estimated at  $7000\text{cm}^2/\text{Vs}$ . The peak width, height, and back-gate position are consistent with single-layer graphene and provide evidence that the electronic structure and degree of disorder of the graphene was not strongly affected by the oxide. Slices at finite  $-VTG$  reveal a doubly-peaked structure. The weaker peak, which remains near VBG  $-2.5\text{V}$  at all VTG, corresponds to the Dirac point of region 1. The stronger peak, which moves linearly with VTG, is the Dirac point for region 2. The difference in peak heights is a consequence of the different aspect ratios of regions 1 and 2.

[079] Horizontal slices through the 2-D plot of Fig. 9A at fixed VBG, corresponding to the horizontal lines in Fig. 9A are shown in Fig. 9B. These slices show a single peak corresponding to the Dirac point of region 2. This peak becomes asymmetric away from the charge-neutrality point in region 1. The changing background resistance results from the different density in region 1 at each VBG setting.

[080] Fig. 9D is a plot of measured current,  $I$  as a function of applied voltage,  $V$ , for the device, measured throughout the (VTG, VBG) plane. This plot indicates no sign of rectification in any of the four quadrants or at either of the charge-neutral boundaries between quadrants, as expected for reflectionless “Klein) tunneling at the p-n interface

[081] A plot of differential conductance,  $g=1/R$ , as a function of VBG and VTG with an applied magnetic field of  $B=4\text{T}$  is shown in Fig. 10A. A vertical slice of data taken at VTG=0 through the p-p and n-n quadrants of the plot of Fig. 10A is shown in Fig. 10B. This plot reveals conductance plateaus at 2, 6, and  $10\ e^2/h$  in both quadrants, demonstrating conclusively that the sample was single-layer and that the oxide did not significantly

distort the Dirac spectrum.

[082] In the quantum hall (QH) regime at large B, the Dirac-like energy spectrum of graphene gives rise to a characteristic series of QH plateaus in conductance, reflecting the presence of a zero-energy Landau level, that includes only odd multiples of  $2 e^2/h$ , that is, 2, 6, 10, ... times  $e^2/h$ , for uniform carrier density in the graphene layer. These plateaus can be understood in terms of an odd number of QH edge states, including a zero-energy edge state at the edge of the graphene layer, circulating in a direction determined by the direction of B and the carrier type. The situation is somewhat more complicated when varying local density and carrier type across the graphene layer.

[083] QH features were investigated for differing filling factors  $\nu_1$  and  $\nu_2$  in regions 1 and 2 of the graphene layer. A horizontal slice through Fig. 10A at filling factor  $\nu_1=6$  is shown in Fig. 10C. Starting from the n-n quadrant, plateaus are observed at  $6 e^2/h$  and  $2 e^2/h$  at top-gate voltages corresponding to filling factors  $\nu_2=6$  and 2, respectively. Crossing over to the n-p quadrant by further decreasing VTG, a new plateau at  $3/2 e^2/h$  appears for  $\nu_2=-2$ . In the  $\nu_2=-6$  region, no clear QH plateau is observed. Fig. 10D provides a plot of data from a horizontal slice at  $\nu_1=2$  in Fig. 10A, showing  $2 e^2/h$  plateaus at both  $\nu_2=6$  and 2. Crossing into the n-p quadrant, the conductance exhibits QH plateaus at  $1 e^2/h$  for  $\nu_2=-2$  and near  $3/2 e^2/h$  for  $\nu_2=-6$ .

[084] For  $\nu_1$  and  $\nu_2$  of the same sign (n-n or p-p), the observed conductance plateaus follow an expression as:

$$g = \min(|\nu_1|, |\nu_2|) \times e^2/h. \quad (\text{B.1})$$

[085] This relation suggests that the edge states common to both regions propagate from source to drain while the remaining —?1-?2— edge states in the region of highest absolute filling factor circulate internally within that region and do not contribute to the conductance. This picture is consistent with known results on conventional 2D electron gas systems with inhomogeneous electron density.

[086] Recent theory addresses QH transport for filling factors with opposite sign in regions 1 and 2 (n-p and p-n). In this case, counter-circulating edge states in the two regions travel in the same direction along the p-n interface, as shown in Fig. 10F, which presumably facilitates mode mixing between parallel-traveling edge states. For the case of complete mode-mixing, that is, when current entering the junction region becomes uniformly distributed among the  $|\nu_1|+|\nu_2|$  parallel-traveling modes, quantized plateaus are expected (18) at values given by the expression:

$$g = \frac{|\nu_1||\nu_2|}{|\nu_1| + |\nu_2|} \times e^2/h. \quad (\text{B.2})$$

[087] A table of the conductance plateau values given by Expressions 1 and 2 is shown in Fig.10E. Plateau values at  $1e^2/h$  for  $\nu_1=1, \nu_2=2$  and at  $3/2 e^2/h$  for  $\nu_1=6$  and  $\nu_2 =-2$  are observed in experiment. Notably, the  $3/2 e^2/h$  plateau suggests uniform mixing among four edge states (three from region 1 and one from region 2). All observed conductance plateaus are also seen at T=4K and for B in the range 4 to 8 T.

[088] There was found some departures between the experimental data and Expressions 1 and 2, as represented in the grid of Fig. 10E. For instance, the plateau near  $3/2 e^2/h$  in Fig. 10D is seen at a value of  $1.4 e^2/h$  and no clear plateau at  $3 e^2/h$  is observed for  $\nu_1 = \nu_2 = 6$ . It was speculated that the conductance in these regions being lower than their expected values is an indication of incomplete mode mixing. Also observed was an unexpected peak in conductance at a region in gate voltage between the two  $1 e^2/h$  plateaus at  $\nu_1=\pm\nu_2=2$ . This rise in conductance is clearly seen for — VTG — values between 1 and 2 V and VBG values between -5 and -2V. This may result from the possible existence of puddles of electrons and holes near the charge-neutrality points of regions 1 and 2, as previously suggested.

[089] These examples demonstrate that graphene p-n junction devices of the invention enable both device operation and the study of physical phenomena in graphene layers.

[090] With this description it is demonstrated that the invention provides carbon-based

structures such as graphene p-n junction devices that can be arranged and controlled to include any number of p-n junctions, including a single p-n junction, with one or more device electrodes on the graphene layer being disposed underneath a top gate. Each region of graphene to be controlled with a selected charge carrier type by a local top gate can be individually contacted if desired. This enables distinct control of p-type and n-type regions, that can be adjacent to each other, and that can be provided even as a single p-n junction device or multiple-junction device or circuit arrangement. Unlike state-of-the-art silicon bipolar electronics, in which ion implantation is used to create fixed p-type and n-type regions having carrier densities that are also fixed, p-type and n-type charge carrier regions, regions of a graphene device of the invention can be temporally and separately controlled to be either n-type or p-type, and can be reversed to the opposite charge carrier type, with precise control over the carrier density, tailored to suit the function of the device. Completely reconfigurable bipolar graphene electronics are thereby provided by the invention. The graphene devices are temperature insensitive, because graphene is itself insensitive to temperature variation, and therefore graphene device operation from 4K all the way up to room temperature, can be achieved with a wide array of p-n junction device and circuit configurations.

[091] Also as demonstrated above, the invention provides a microfabrication process for producing carbon-based structures, such as graphene p-n junction devices and circuits, with a technique for functionalizing a carbon surface prior to gate oxide formation. The functionalization layer blanket-coats the carbon surface to prevent extrinsic doping of the surface by the ambient environment, and enables the growth of a wide variety of top gate oxide layers, including ferroelectric and ferromagnetic layers, without altering the electronic properties of the undoped graphene. The invention provides an electron beam rastering process to compensate for any extrinsic doping of a carbon surface that occurs during microfabrication processing. The electron beam rastering process enables the production of carbon-based structures, such as graphene devices and circuits, that are electrically robust

and exhibit reproducible performance characteristics. It is recognized, of course, that those skilled in the art may make various modifications and additions to the devices, circuits, and microfabrication processes of the invention without departing from the spirit and scope of the present contribution to the art. Accordingly, it is to be understood that the protection sought to be afforded hereby should be deemed to extend to the subject matter of the claims and all equivalents thereof fairly within the scope of the invention.

## B.8 Claims

[092] We claim:

1. A method for forming a material layer on a carbon structure comprising: exposing a carbon surface of the carbon structure to at least one functionalization species that non-covalently bonds to the carbon surface while providing chemically-functional groups at the carbon surface; and exposing the chemically-functionalized carbon surface to a beam of electrons to compensate for extrinsic doping of the carbon surface.
2. The method of claim 1 wherein exposing the chemically-functionalized carbon surface to a beam of electrons comprises rastering a beam of electrons across the carbon surface.
3. The method of claim 1 further comprising, before exposing the chemically-functionalized carbon surface to a beam of electrons, exposing the chemically-functionalized carbon surface to at least one material layer precursor species that deposits a material layer on the chemically-functionalized carbon surface.
4. The method of claim 1 wherein the carbon surface comprises a surface of a layer of graphene.
5. The method of claim 1 wherein the carbon surface comprises a cylindrical wall of a carbon nanotube.
6. The method of claim 1 wherein the functionalization species comprises NO<sub>2</sub>.
7. The method of claim 1 wherein the functionalization species comprises a precursor se-

lected from the group consisting of trimethylaluminum and tetrakis(dimethylamido)hafnium.

8. The method of claim 1 wherein the functionalization species comprises NO<sub>2</sub> and tetrakis(dimethylamido)hafnium.

9. The method of claim 1 further comprising forming a layer of oxide on the chemically-functionalized carbon surface before exposing the carbon surface to a beam of electrons.

10. The method of claim 9 wherein forming a layer of oxide comprises forming a layer of HfO<sub>2</sub>.

11. The method of claim 1 wherein exposing a carbon surface of the carbon structure to at least one functionalization species comprises atomic layer deposition of a functionalization species on the carbon surface.

12. The method of claim 11 further comprising forming a layer of oxide on the chemically-functionalized carbon surface by atomic layer deposition.

13. A method for forming a material layer on a graphene layer comprising: exposing a surface of the graphene to at least one functionalization species that non-covalently bonds to the graphene surface while providing chemically-functional groups at the graphene surface; forming a layer of oxide on the chemically-functionalized graphene surface; and exposing the layer of oxide and the chemically-functionalized graphene surface to a beam of electrons to compensate for extrinsic doping of the carbon surface.

14. A structure comprising: a carbon material; and a layer of HfO<sub>2</sub> disposed on a surface of the carbon material; wherein the carbon material is electrically undoped.

15. The structure of claim 14 wherein the carbon material comprises a layer of graphene.

16. The structure of claim 14 wherein the carbon material comprises a carbon nanotube.

17. The structure of claim 14 further comprising a functionalization layer, under the HfO<sub>2</sub> layer, that is non-covalently bonded to the carbon material surface and that provides chemically functional groups bonded to the HfO<sub>2</sub> layer.

18. A graphene p-n junction device comprising: a graphene layer; a backgate electrode connected to a first surface of the graphene layer; a first device electrode connected to a

first region of the graphene layer; a second device electrode connected to a second region of the graphene layer; a dielectric layer blanket-coating the second graphene surface and the device electrodes; and a top gate electrode disposed on the dielectric layer over one of the device electrodes.

19. The device of claim 18 further comprising a second top gate electrode disposed on the dielectric layer over a second one of the device electrodes.

20. The device of claim 18 further comprising a functionalization layer, under the dielectric layer, that is non-covalently bonded to the second graphene surface and that provides chemically functional groups bonded to the dielectric layer.

21. The device of claim 20 wherein the functionalization layer comprises NO<sub>2</sub> and a species selected from the group consisting of trimethylaluminum and tetrakis(dimethylamido)hafnium.

22. The device of claim 18 wherein the dielectric layer comprises an oxide selected from the group consisting of Al<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>, and ZrO<sub>2</sub>.

23. The device of claim 18 wherein the graphene layer is disposed on a substrate, on top of a layer of oxide coating one surface of the substrate.

24. The device of claim 23 wherein the substrate comprises a silicon wafer.

25. The device of claim 23 wherein the substrate forms the backgate electrode.

26. The device of claim 18 wherein the first and second graphene regions form a circuit wiring connection between device electrodes.

27. The device of claim 18 wherein the first and second graphene regions form a single p-n junction with one p-type region adjacent to one n-type region.

28. The device of claim 18 wherein the graphene layer includes a plurality of p-n junctions.

29. The device of claim 18 further comprising a third device electrode connected to a third region of the graphene layer.

30. The device of claim 18 further comprising at least three device electrodes connected to corresponding regions of the graphene layer.

31. The device of claim 18 further comprising a plurality of top gate electrodes disposed on the dielectric layer over corresponding device electrodes.

32. The device of claim 18 further comprising a third device electrode connected to a third region of the graphene layer and a second top gate disposed on the dielectric layer over a second one of the device electrodes.

## **B.9 Figures**

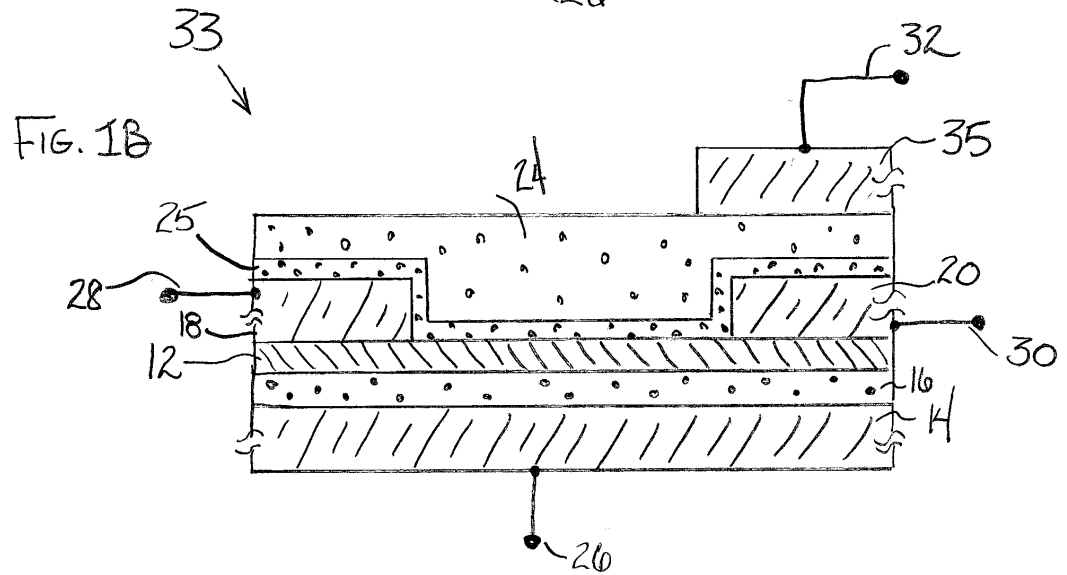
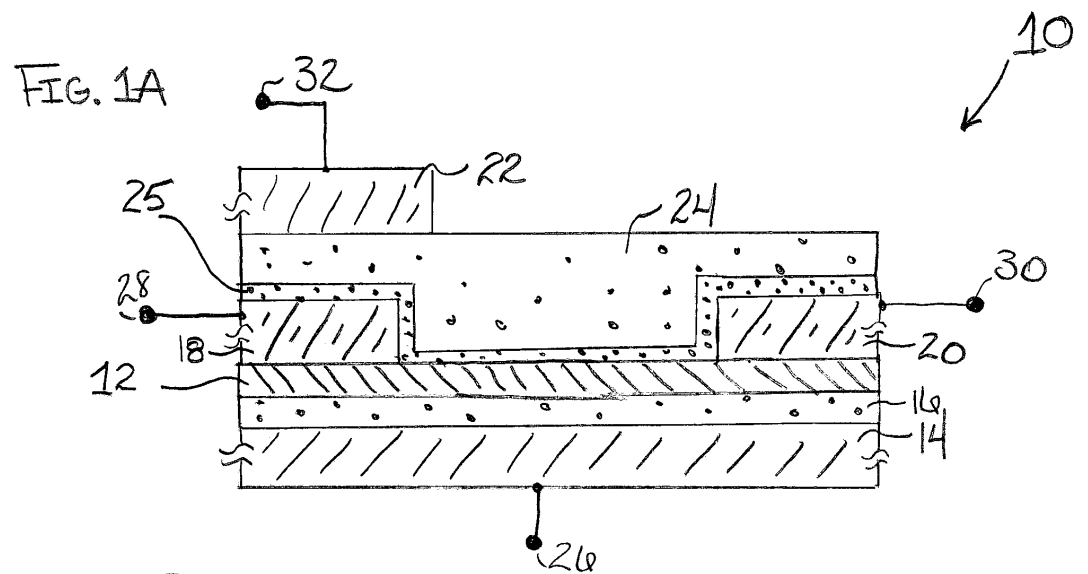


FIG. 2A

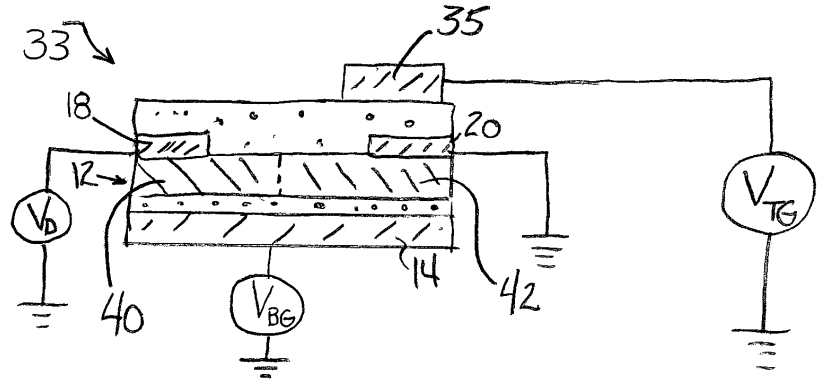
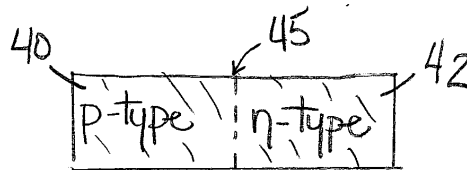
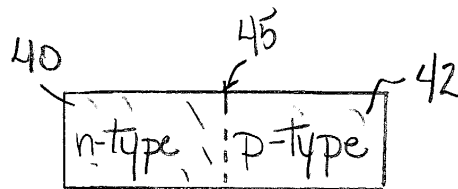


FIG. 2B



$$V_{BG} < 0; V_{TE} > 0 + \frac{C_{TE}}{C_{BG}} V_{BG}$$

FIG. 2C



$$V_{BG} > 0; V_{TE} < 0 + \frac{C_{TB}}{C_{BG}} V_{BG}$$

FIG. 3A

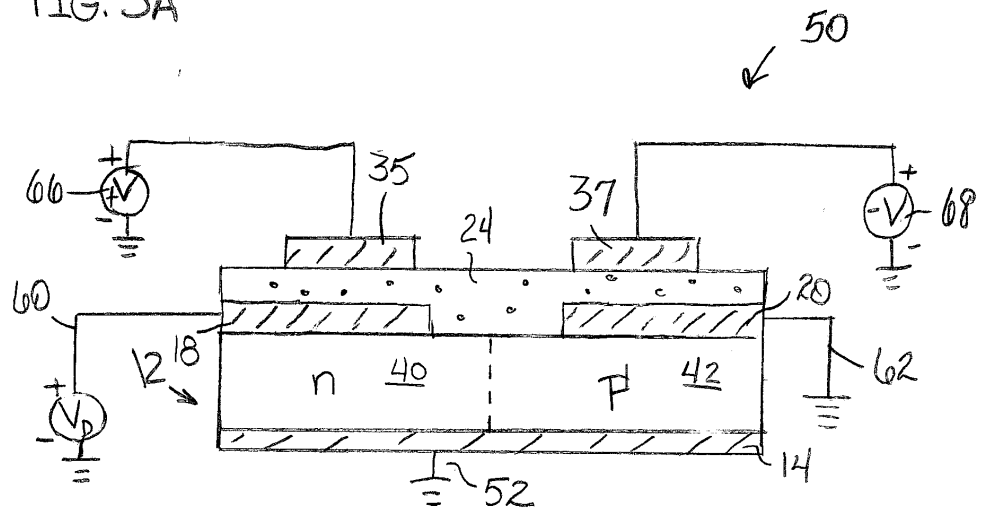


FIG. 3B

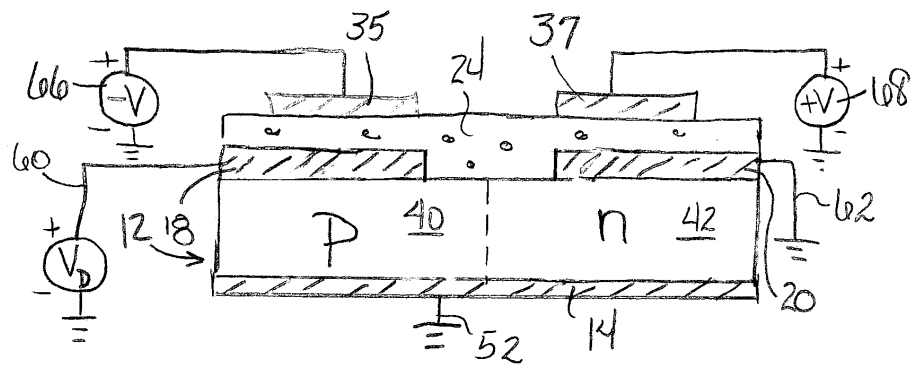


FIG. 3C

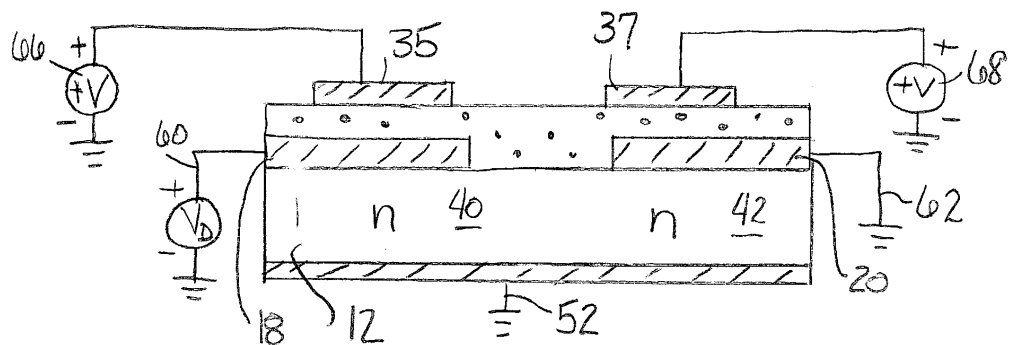


FIG. 4A

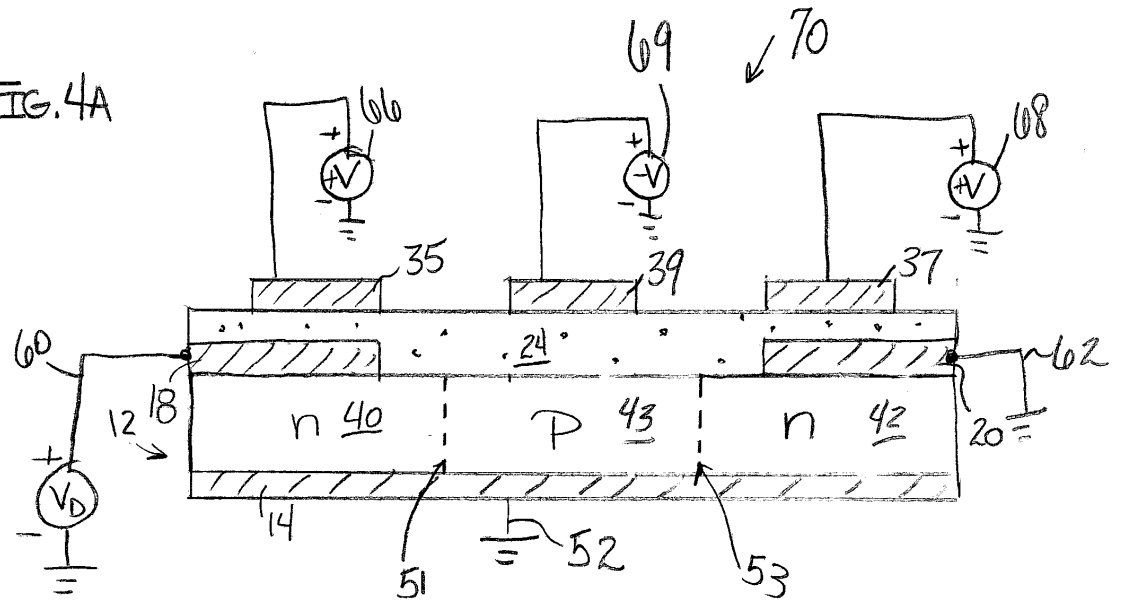


FIG. 4B

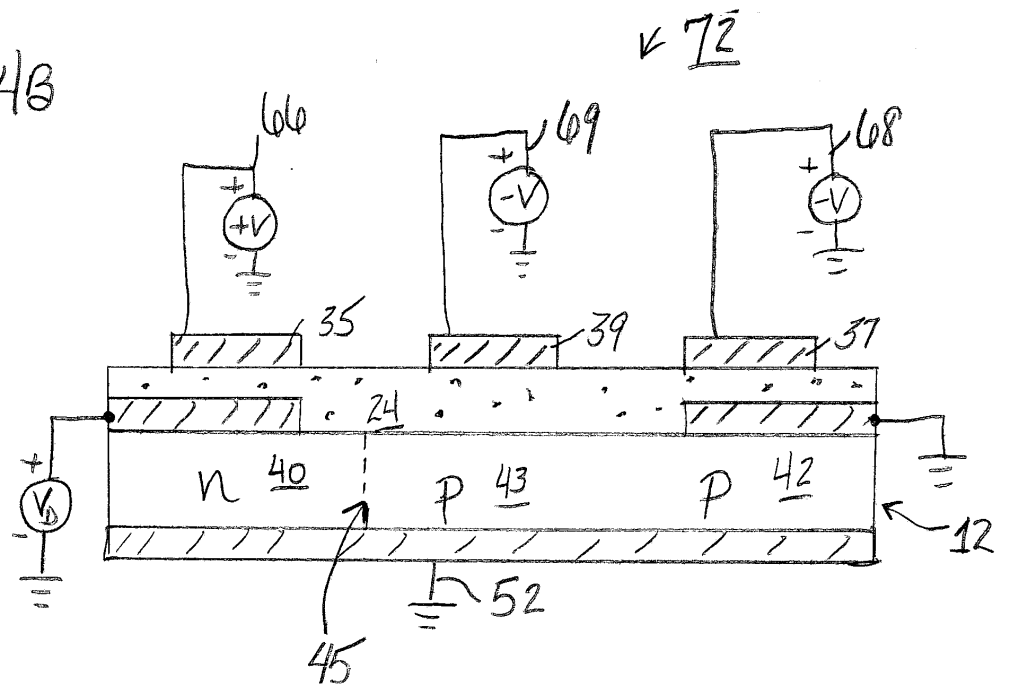


FIG. 4C

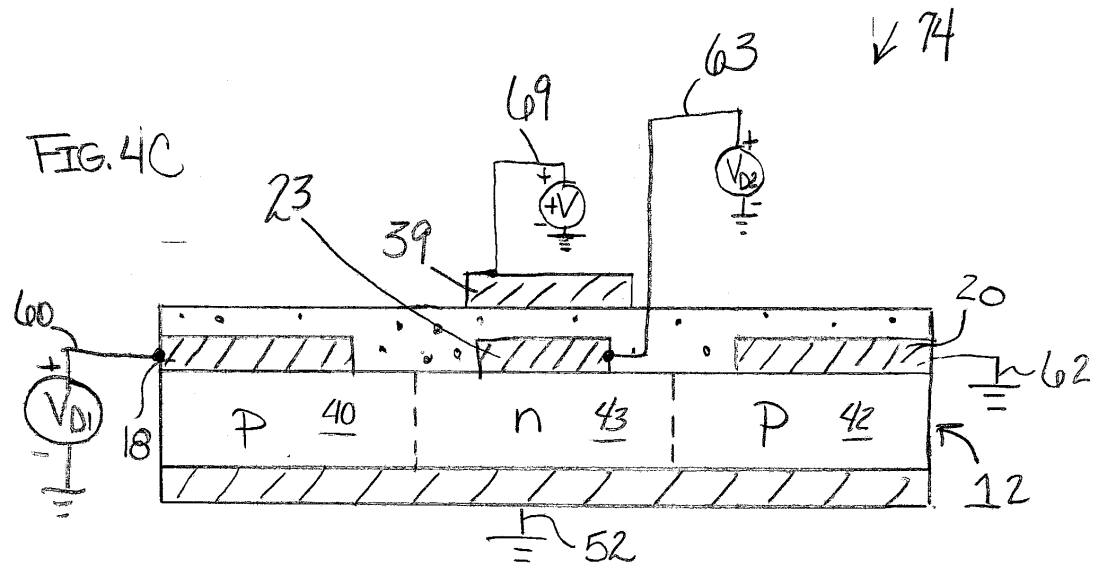


FIG. 4D

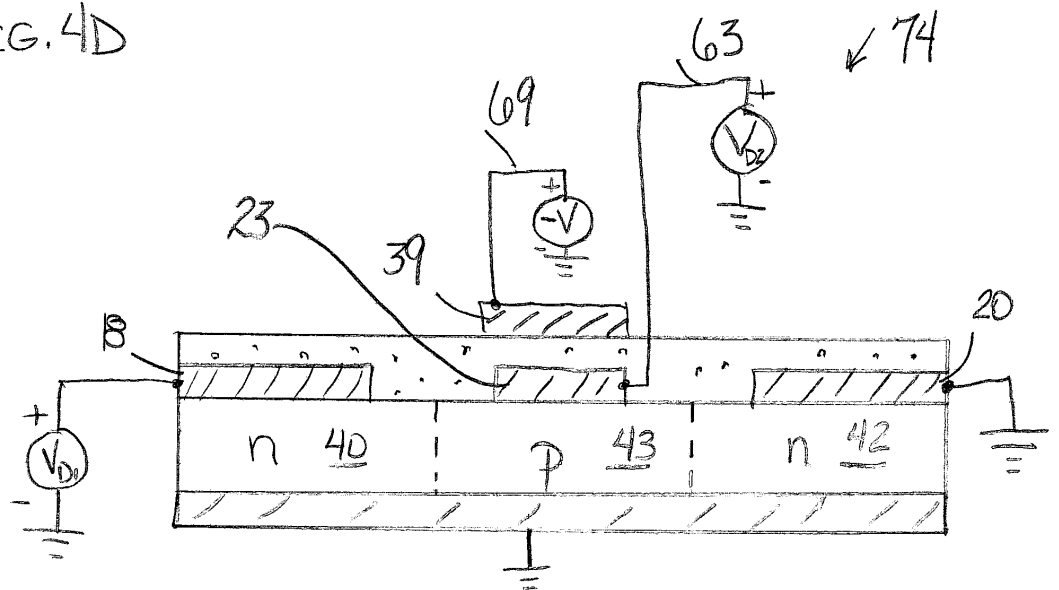


FIG. 5A

$$V_{TG,p} \equiv -V$$

$$V_{TG,n} \equiv V$$

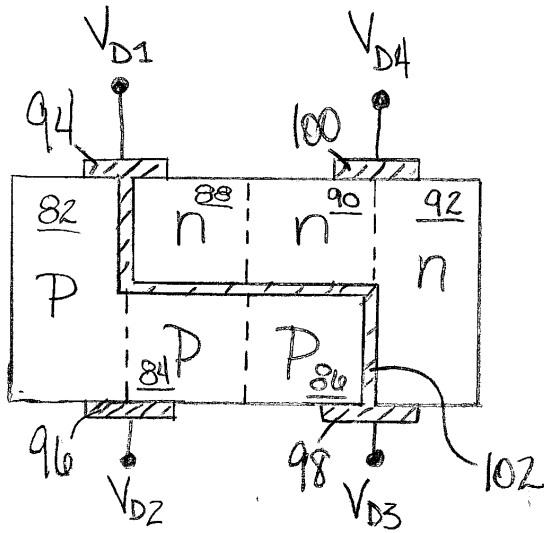


FIG. 5B

$$V_{TG,p} \equiv -V$$

$$V_{TG,n} \equiv V$$

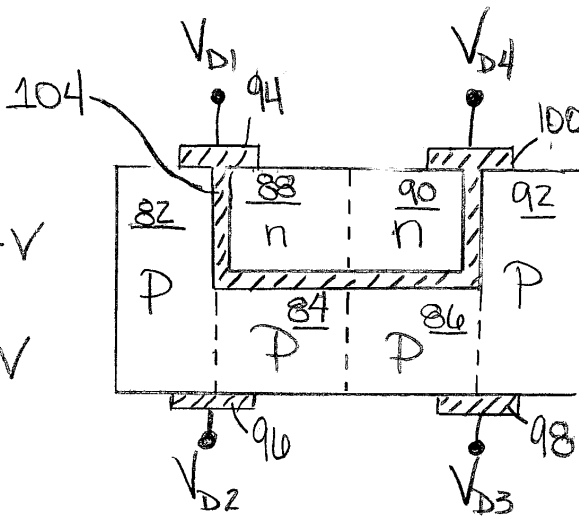


FIG. 6

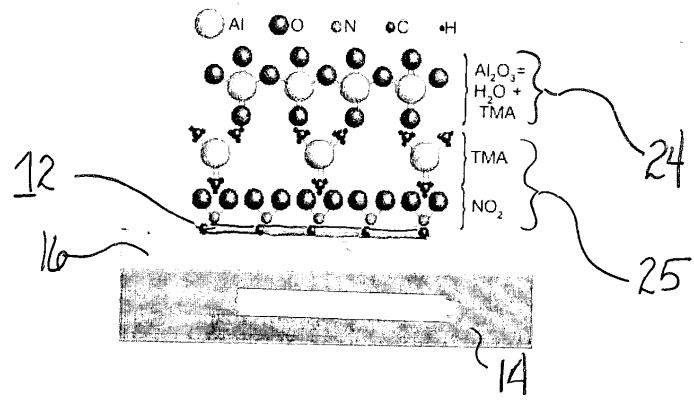


FIG. 7

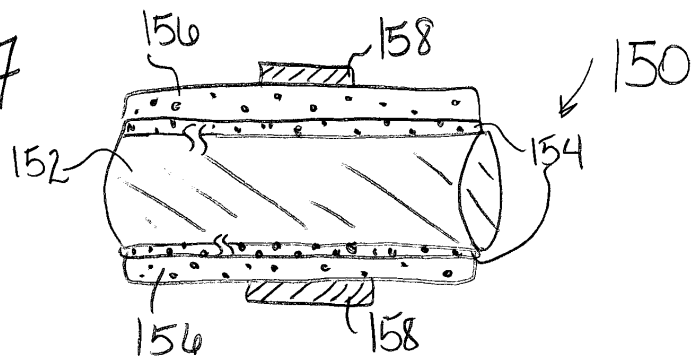


FIG.8A

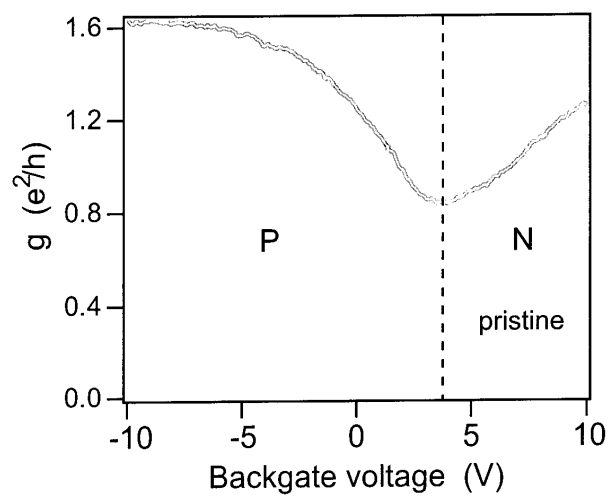


FIG.8B

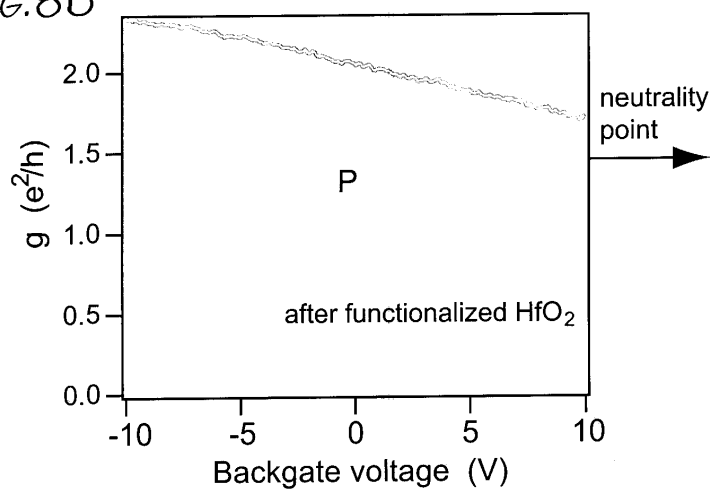


FIG.8C

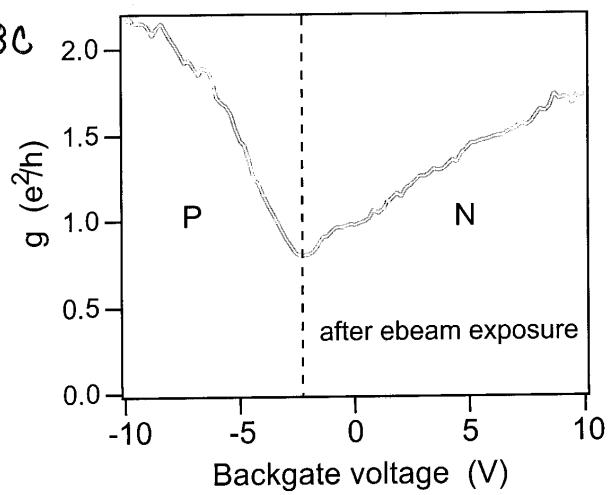


FIG. 9A

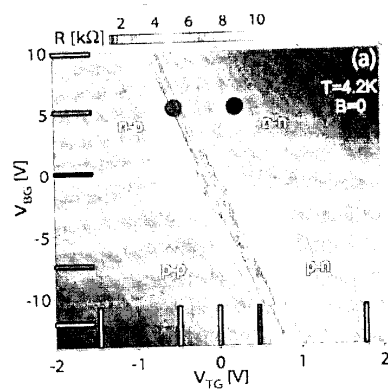


FIG. 9B

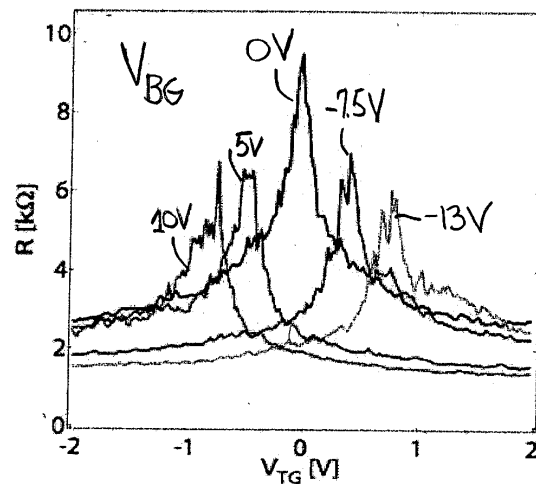


FIG. 9C

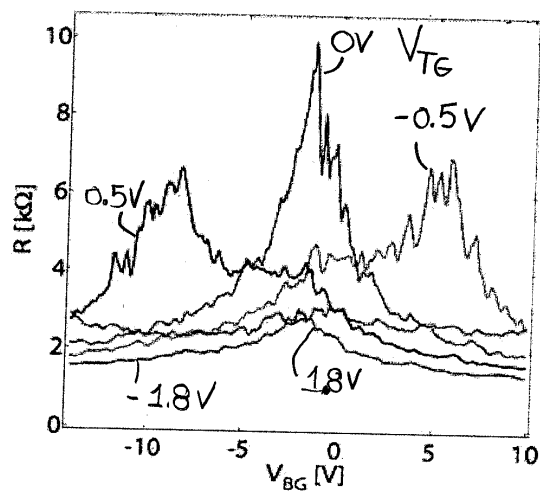


FIG. 9D

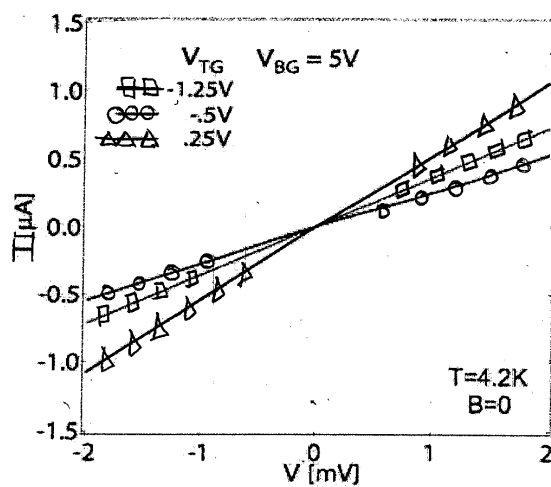


FIG. 10A

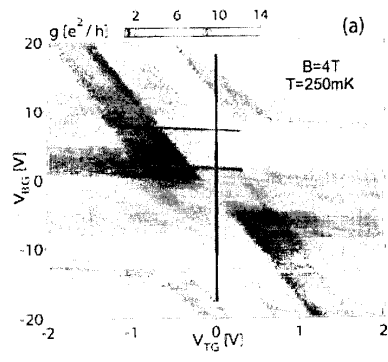


FIG. 10B

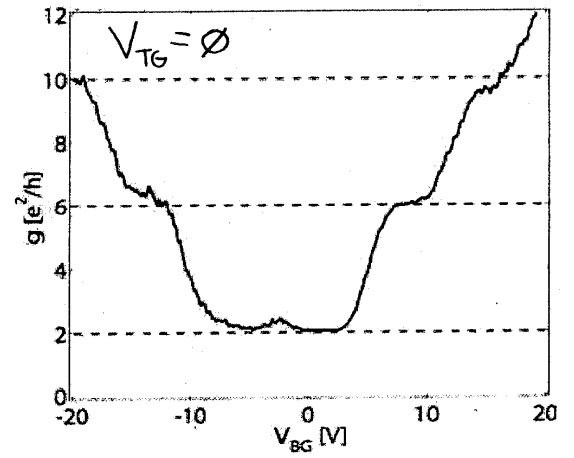


FIG. 10C

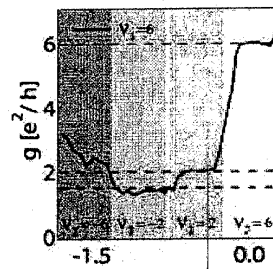


FIG. 10D

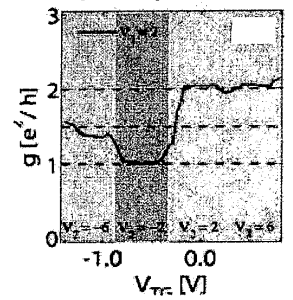


FIG. 10E

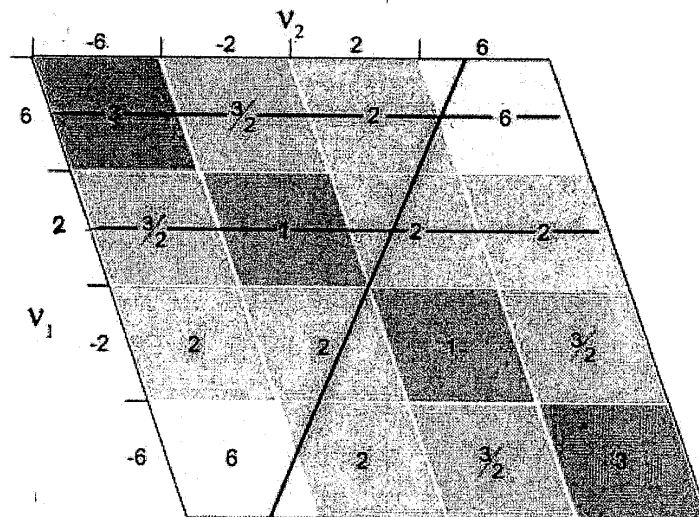
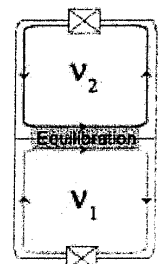


FIG. 10F



## Appendix C

# Elionix 7000 User Guide

The first step is to take the .dxf file you created in DesignCAD or any other CAD software and convert it into the file type that Elionix uses, called a .CEL file. To this, open the dxfTOcel DOS window and perform the following.

- Open new command shell (DOS) by typing cmd into Run window
- Type cd desktop
- Type dxfcel or gds2cel (choose the one that is appropriate for your file type)
- Enter filename that is on the desktop
- Enter name you want the .CEL file to be
- Enter units of your drawing (choose 0 for mm and 1 for microns)
- Do you want to specific layers? If yes, make sure your layers are named with 1, 2 in the CAD program
- Arc division? No
- Elliptic Arc? No
- Arc in Polygon? No
- Paint? Yes
- Way of painting ellipse? 1 Pitch? 0.1 (Depends on your preference)
- Dose Conversion? No - Choose the layer number you want to convert by: 1,2,4

Choose the appropriate sample holder (see Fig. 2). Load the sample on the sample plate. Do not use metal tweezers or anything that will scratch the metal surface. Make sure the sample is secure and that it is flat against the sample holder.

- Make sure the Elionix is in the right position to load the sample. To do this, press the EX button on the Stage Controller (Fig. 4). If you can't find the Stage Controller,

```

C:\WINDOWS\system32\cmd.exe
Microsoft Windows XP [Version 5.1.2600]
(C) Copyright 1985-2001 Microsoft Corp.

C:\Documents and Settings\Jimmy>cd desktop
C:\Documents and Settings\Jimmy\Desktop>dxfccl

*** DXF Conversion Program (Version 2.82) ***

DXF file name :L0AlignSmall
CEL file name:L0AlignSmall
unit ? (0:mm/1:micron):1
Do you want to specify layers ?(y/n) : n
Arc division(unit:degrees 0:CPG) : n
Elliptic Arc division(unit:degrees) : n
Arc in Polygon division(unit:degrees) : n
paint ?(y/n): y
the way of painting ellipses (0:line/1:rectangle) : 1
the pitch (micron): 0.1
Dose conversion? (y/n) : n

DXF Version [Release14]
EOF : Number of records (DXF file) : 6514

*** Completed Conversion ***

C:\Documents and Settings\Jimmy\Desktop>

```

Figure C.1: Command Prompt for the DXF to CEL conversion.



Figure C.2: Choices of sample holders. Cassette for small piece used in this manual.

see the last section of this manual “Where is everything?”. Wait until the red light on the Stage Limit panel turns on before proceeding.

- Close the isolation valve by pressing the green “Open” button and holding it for 2 seconds (see Fig. 5). You will hear a noise when the isolation valve closes.

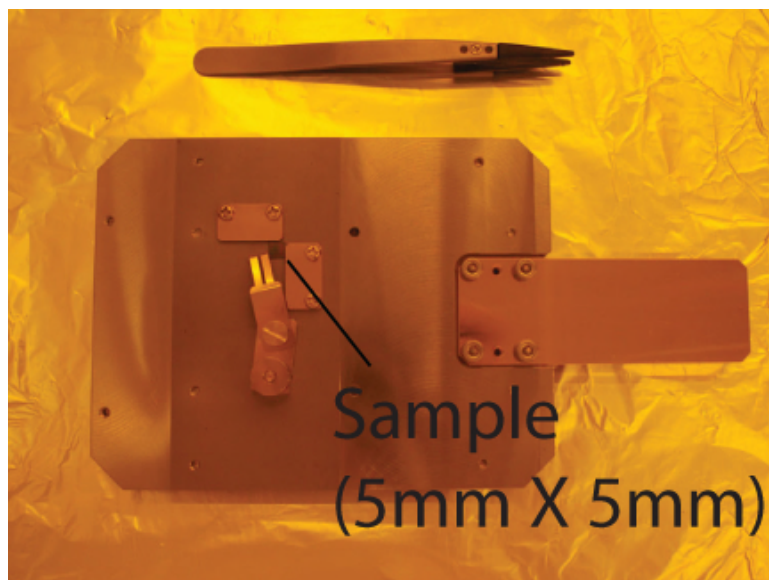


Figure C.3: Small piece sample holder shown with 5mm by 5mm sample. **Do not use metal tweezers or anything that will scratch the surface of the sample holder.**

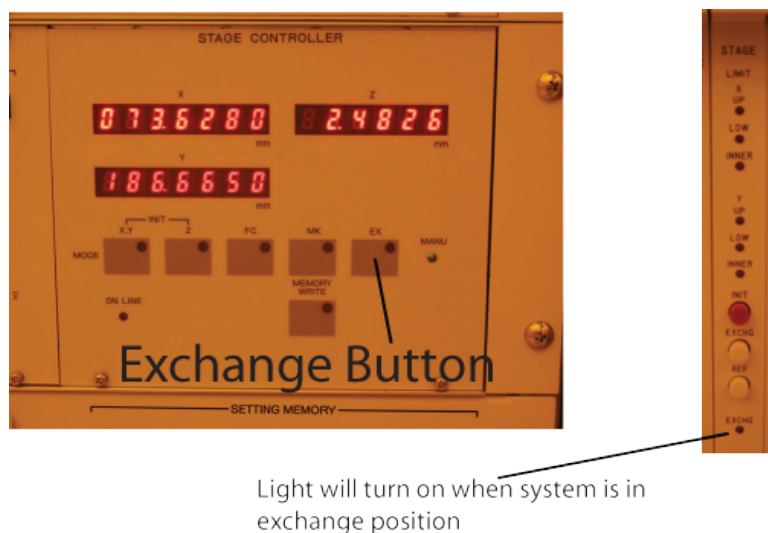


Figure C.4: To ready the Elionix for sample loading, press the Sample Exchange button on the Stage Controller. Wait until the red light comes on in the Stage Limit before proceeding.

- Vent the load by toggling Vacuum Toggle Button to vent (see Fig. 6). Make sure the gate valve door is closed before venting the loadlock.
- When the vent the loadlock is a atmosphere, it will automatically open. Insert the sample plate into the loadlock as shown in Fig. 7 and screw the transfer rod into the sample plate. Don't tighten the screw too much; once it reaches its maximum, pull

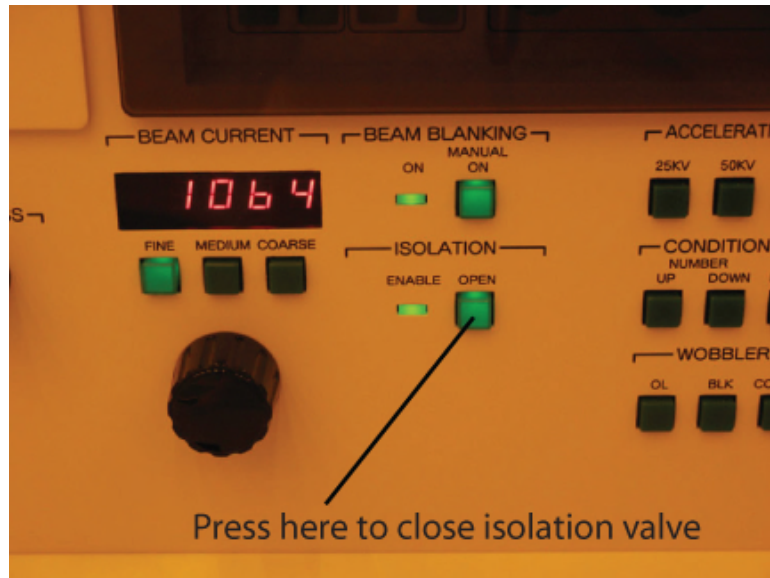


Figure C.5: Make sure the isolation valve is closed before venting the loadlock.



Figure C.6: To vent the loadlock, turn the toggle switch to vent. **Make sure the Door Control Button is set to closed.**

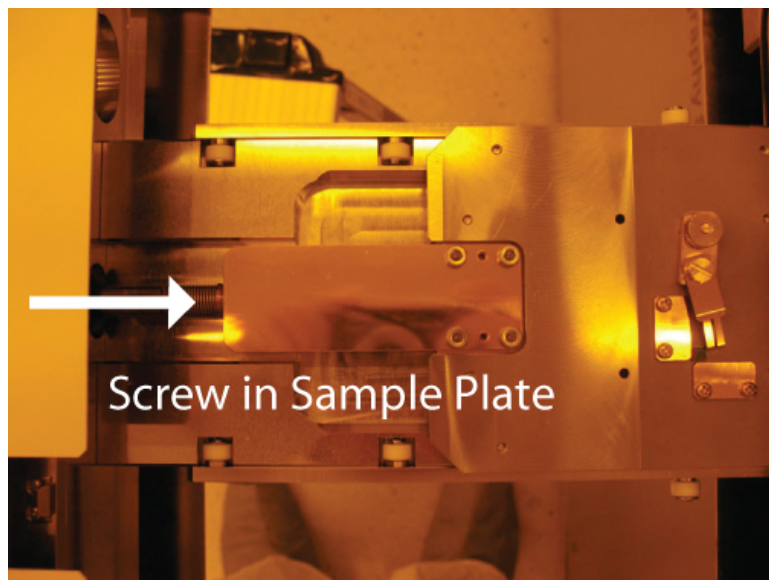


Figure C.7: Load sample plate into the loadlock.

back 1/2 a turn.

- Close the loadlock and switch the Vacuum Toggle Button to Evac.
- Once the loadlock is pumped down to an appropriate pressure, the Evac light will cease blinking and will remain solid green. Then and only then can you switch the Door Control Button to Open. While doing this, place your hand on the transfer rod to prevent the sample plate from being pulled into the main chamber.
- When you flip the Door Control Button, wait for two sounds before attempting to insert the sample plate. Once the gate valve has fully opened, turn the transfer rod lock button 1/2 turn counterclockwise to release the rod (see Fig. 8) and move the transfer rod all the way in.
- Insert the sample all the way into the chamber until the transfer rod is fully extended. Turn the rod counterclockwise until the white stripe on the rod has the same width as the white stripe (see Fig. 9). Give the rod a few more turns to be sure the screw is not longer attached to the sample plate and then fully retract the transfer rod.

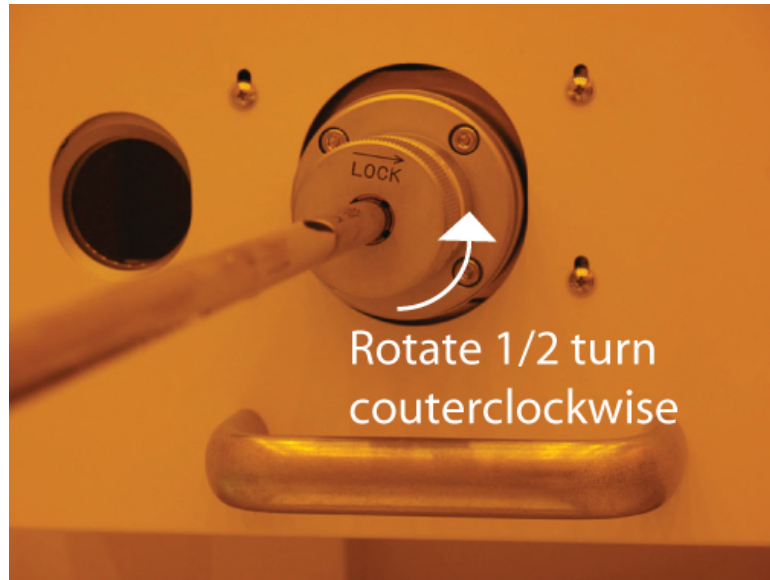


Figure C.8: Transfer Rod Lock.



Figure C.9: Make sure the two white stripes have the same width before retracting the transfer rod.

- Close the gate valve by switching the Door Control Button to “Close”.
- Lock the transfer rod into place. Close the gate valve by toggling the Door Control Button to CLOSE.

You are now ready to get everything set up. This includes setting and measuring beam

current and adjusting focus and stigmation.

First, open the isolation valve by pressing and holding the Isolation Open Button for 2 seconds (see Fig. 5). Then press the FC (Faraday Cup) on the stage controller to drive the sample to the Faraday Cup (The FC button is located 2 buttons to the left of the EX button on the Stage Controller, see Fig. 4). To set the current, perform the following

- Using the Condition Memory inputs and the Memory Settings Display (see Fig. 10), set the current you desire. There are 3 values for current preset into the memory. They are: Setting 1 (20pA), Setting 2 (100pA), and Setting 3 (2nA). Setting 4 - 9 are available to users to set their own values. To set a current, use the up/down buttons to select the appropriate memory element. Once the appropriate element is chosen, press the Call button twice to change the current. Once you press the call button twice, the Setting Memory Window should now reflect the values you just chose. Also, the beam current display (to the left of the Condition Memory inputs) should now reflect the value you entered. You can enter the current settings into a memory element (use only 4-9, don't touch 1-3) by pressing the enter button twice.
- To measure the current, first un-blank the beam using the Beam Blanking Manual On Button (see Fig. 11A). When the current light under the button is off it means the beam is not blanked. Next, using the Magnification knob (Fig. 11B), zoom out until you are at 200 or 400 X magnification (the Current Status menu will display the current Magnification). You should now see an image similar to the one shown in Fig. 11D. Center the FC in the image using the Stage Driver (Fig. 11C) and zoom in to 100kX. The Pico Ammeter should now read the current (Fig. 11E). If not, try adjusting the current range using the up/down buttons at the bottom left of the Pico Ammeter.

To set focus and stigmation, first drive to the Ref position using the bottom button of



Figure C.10: Elements used in setting up the beam current.

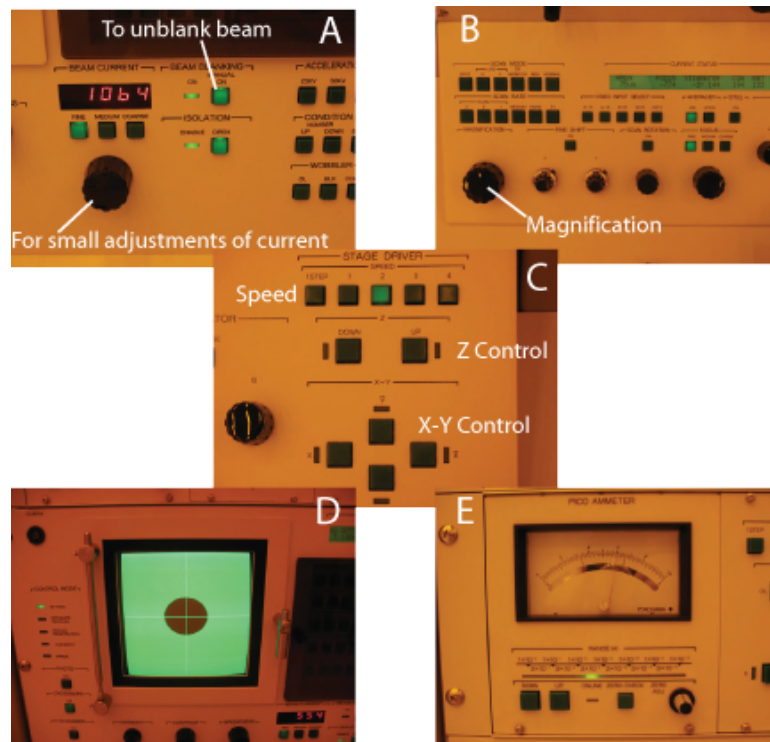


Figure C.11: Elements used in reading the beam current.

the Stage Limit controller (see Fig. 4, right). The stage will drive to the Ref position and it will attempt to set the focal height using the laser position monitor. Wait until you hear

two beeps which indicates that the process is complete. If you unblank the beam now, you will see an image similar to Fig. 12A, which has a black strip in the center of two gold pads.

- Zoom in to 200-400kX and use the focus and stigmation to sharpen the image of the gold islands. When the focus and stigmation are correct, the gold islands should appear clear and sharp (see Fig. 12B).
- Go back to the FC and measure current again to make sure the value is still what you want.
- Press the appropriate value of voltage under the Accelerating Voltage (right above Condition Memory in Fig. 10, 100kV used here) to reset the voltage. Once voltage is reset, the current should still be set to what you want.
- The stage height should now be  $\sim 2.5\text{mm}$  now. Using the Stage Driver, drive to the center of your chip (you can find the center by finding the lower left hand corner of your chip and extrapolating to the center. For my chip, the lower right hand corner is usually around (116mm, 116mm)) and use the Z Control to raise lower the stage to bring your chip into focus. The value of the laser monitor should be 0 (see Fig. 12B) when your chip is in focus and won't come on until your chip is in reasonable focus ( $\sim 3.4\text{mm}$  for my chips that are  $\sim 1\text{mm}$  in height). 5mm X 5mm is on the lower end of when the laser can effectively measure the chip height and the chip needs to be flat against the sample plate for this method to work.

Your sample should now be in focus and you are ready to write.

Using the interface computer, open the ELC Program. A window shown in Fig. 13 will open. We actually start with Job 2, instead of the logical Job 1.

Highlight Job 2 and click EXEC. In Job 2, you can set the Chip size (the same as the write field size on the Raith) which sets the size of the write field that the system can expose without moving the stage. Use small Chip sizes for high resolution lithography. In

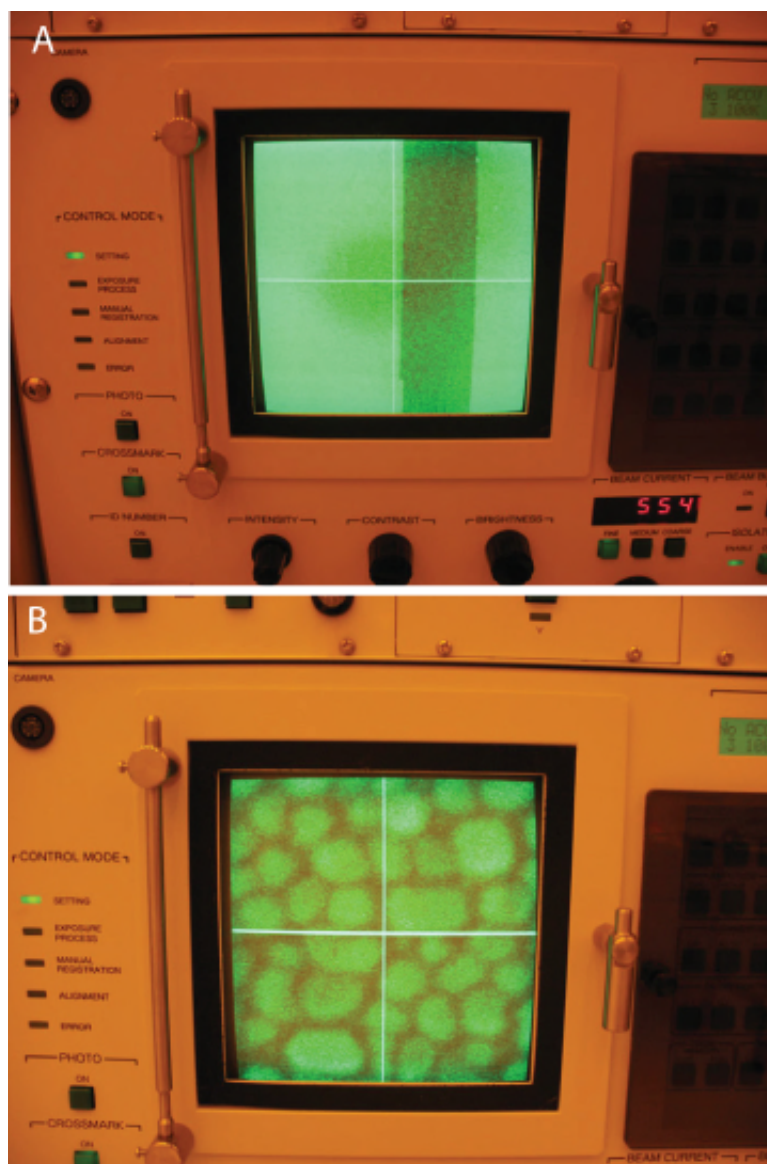


Figure C.12: In the Ref position, use the Au island to set focus and stigmation.

In addition, you can set the Dot Map (equivalent to the step size on the Raith) which sets the number of points that the Chip size is broken up into. If you set the Chip size to 300 and the Dot Map to 20000, your pattern will be exposed in dots that are separated by 15nm. See Fig. 14 for a screen shot of the Job 2 menu. Once you've highlighted the values you want to use, click SAVE.

In Job 1, you will take your .CEL file created in in the .dxf to .cel conversion and turn

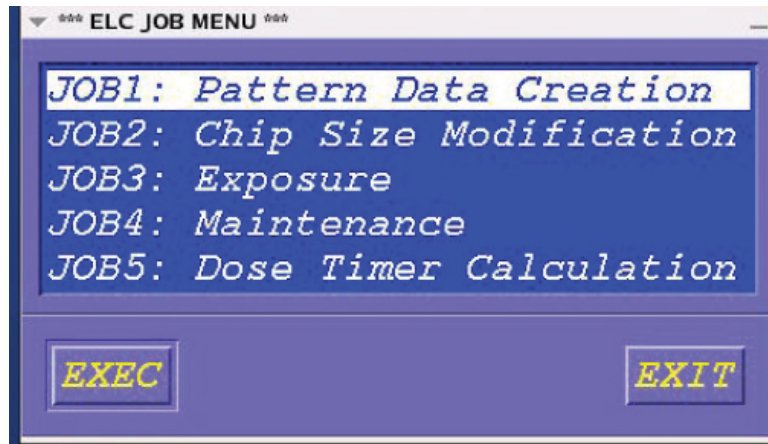


Figure C.13: Opening menu to the ELC program.

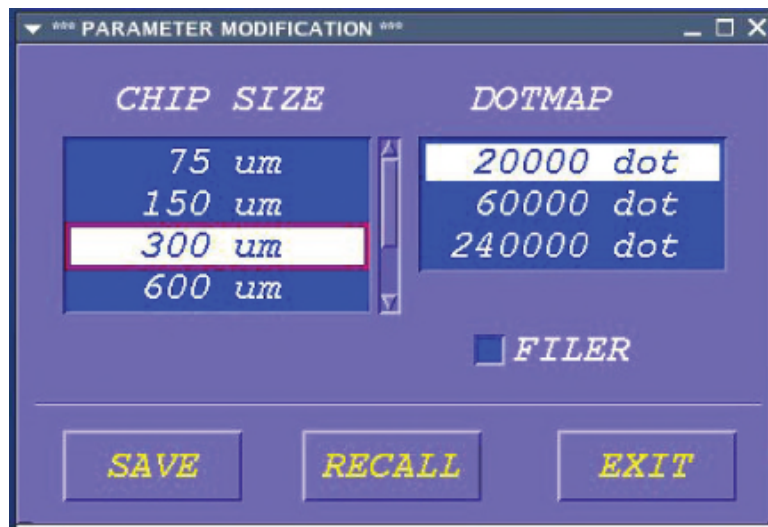


Figure C.14: In Job 2 you can set the Chip size and Dot Map for your write.

in into a file that can be used to do the actual exposure. By the end, you should have a .CON file that has all the positions and geometries of the write you are about to perform.

- Go to the Home menu of the ELC by clicking EXIT in the Job 2 menu.
- Two windows will open: the left one (called the Message Window) allows you to open .CEL file, position your drawings, etc. The right window (called the Graphics Window) will display the files, chip and Registration Marks that you have loaded. The right window contains a display of the entire stage drive area (see Fig. 15A) .

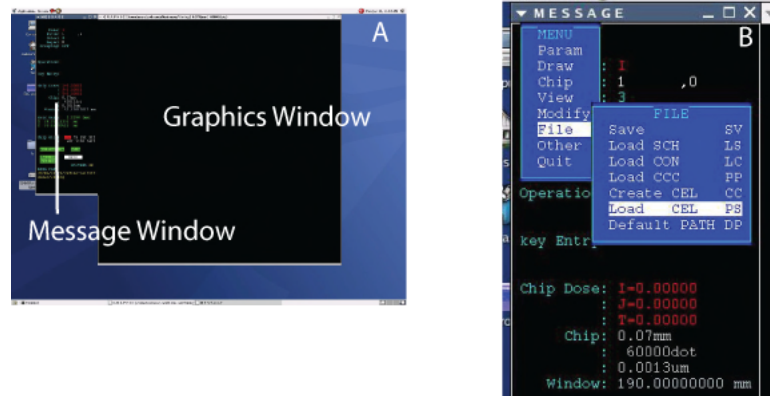


Figure C.15: Loading the .CEL file into the Graphics Window.

- Left click in the message window and choose File → Load .CEL (Fig. 15B).
- The software will then ask you where you would like to place the CAD drawing origin (defined in you CAD program) on the Graphics window. For example, the lower right corner of my chip is  $\sim (116\text{mm}, 116\text{mm})$ . When I want to write my alignment pattern (which covers the whole 5mm X 5mm chip) I place the origin of my drawing at  $\sim (111.3\text{mm}, 116\text{mm})$ . If you would like to specific the point in mm, you need to include a . in every number. For example, for the 116 in the y-coordinate above, I would enter it as 116., this distinguishes it from a dot coordinate, which uses dot count to identify where to put the pattern. For 111.3mm I can enter it just as 111.3, that is, I don't need to write 111.3. . Once you give the coordinates to place your origin, your design will appear in the Graphics Window. You can zoom in and zoom out in the Graphics window by pressing i (zoom in) or o (zoom out) on the keyboard and left clicking on the area you would like to zoom in or zoom out on.
- Next, you need to “Place Chips”, that is define the fields (size determined in Chip Size in Job 2) that you will write your pattern. If you need to write something that is equal to or less than the set Chip Size, you can use the Place Chip command (left click in the message window → Chip → Place Chip) and you will be asked to save the .CCC file (we will call it chipTest.ccc) created when you place the chip. The software

will then ask you to identify the center of where you would like to place the chip. For example, If I would like to place a chip at 111.6mm and 116mm I would enter 111.6, 116. for the coordinates (for more on the Coordinate System, see page 11 of the Elionix user manual). More likely, your CAD drawing will be bigger than your Chip size. In this case, you need to define a chip matrix by left clicking in the Message Window → Chip → Matrix Chip 2. You can then left click on the lower left corner of your loaded .CEL file followed by the left clicking on the upper right corner of your drawing. Then you are prompted ALL "chipTest" (Y) → which you should say N (type N then press Return). Next x-direction (Y)? (Which asks if you want to write in the x-direction first). Then Auto Reverse (Y)? (Which asks if you want to write from left to right on the first line, followed by right to left on the second line). This will create a matrix of chips that should encompass your entire CAD drawing (see Fig. 16A).

- Now, you may want to align a pattern with a pattern that you've already defined on a chip. This works best with patterns that you created using the Elionix (if you're using another machine, please see the Manual, page 76, S correction function). To do this, you'll need to input 2 Registration marks that, prior to exposure, you will either automatically or manually align. This allows for any rotation of the pattern with respect to the global x-y coordinate system to be corrected for (this is similar to setting the u-v coordinate system on the Raith). To enter these two marks, left click in the Message Window select Chip → Reg-2 Mark. Then enter the coordinates of the two marks when prompted. The two markers should appear in the Graphics Window at the position you specified (Fig. 16B).
- Finally, create the .CON file by left clicking in the Message window and selecting File → SAVE and entering the .CON file name into the prompt.

Finally, on to the exposure. Select exposure by choosing Job 3 in the ELC menu. Once

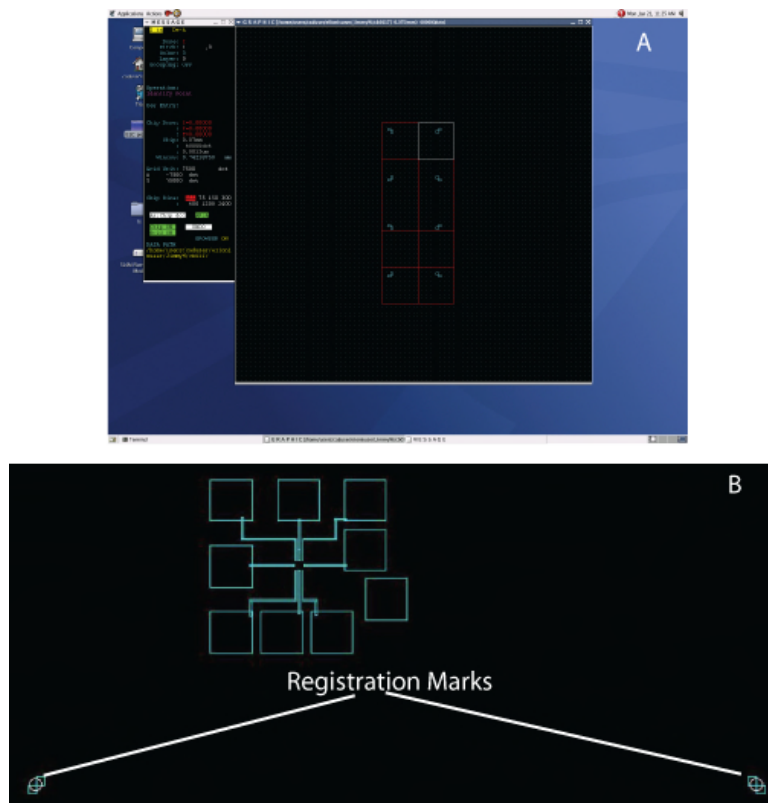


Figure C.16: (A) Chip matrix (red) defined for the .Cel pattern (blue). (B) Once Registration marks are entered, they should appear as white circles around the area you specified.

the program is open, you will see a window consisting of Schedule File Name, Schedule List, Exposure Conditions and Command Explanation (Fig. 17).

- First, set the Exposure Conditions by pressing c on the key board. Fig. 18 shows the recommended exposure conditions (see page 43 of the manual for an explanation of all the fields). For the Exposure Condition Theta Correction, you need to type in the work **theta** to use the file called “theta” used to perform the Theta Correction.
- Second, press “T” (on the keyboard) to insert a .CON file into the Schedule List. Under No Condition, enter the .CON file name. For Position Shift, enter the amount in mm that you want to shift the drawing from the coordinates you entered in Job 1. If you want to write the drawing exactly where you positioned it in Job 1 , enter 0,0 for the x and y position shifts. The position shifts become useful when you are doing

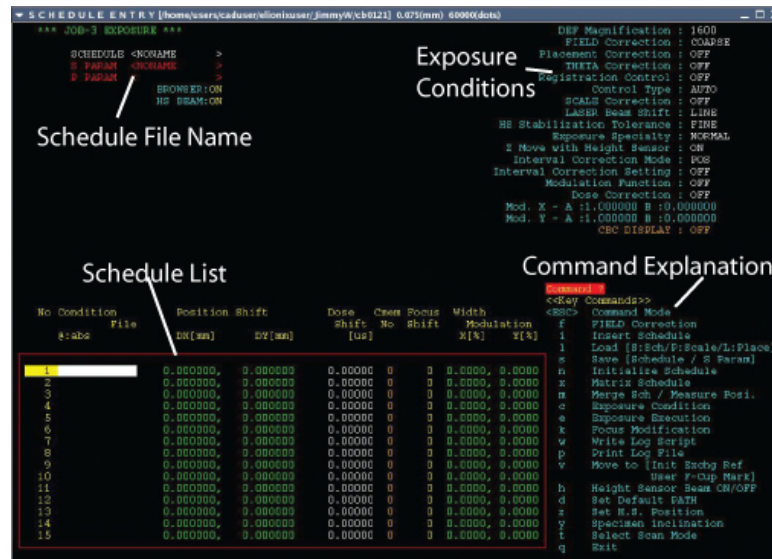


Figure C.17: The home screen of Job 3 Exposure.



Figure C.18: Enter the exposure conditions here.

a dose test and you want to make a matrix of dose (the best way to make a matrix is by typing x and using the Matrix Schedule command). Dose shift allows you to enter the dose (in  $\mu\text{sec}$  per dot). You can calculate this using Job 5 and can enter the value

```
SCHEDULE <NONAME      >
S PARAM  <NONAME      >
P PARAM  <              >
          BROWSER:ON
          HS BEAM:ON

FIELD Correction [COARSE]
FIELD Correction is Completed
Width ATTX : 7992
           Y : 8047
           SRT [mrad]: -1.57
RightAngle [mrad]: -4.27
Elapsed Time [s]: 155

Retry (Y/N) ?
```

Figure C.19: Display after Field Correction is complete.

here. Try to keep the dose time above  $.5 \mu\text{sec}$  per dot to avoid exposure areas (going below this can cause a burnout of some electronics that control the beam blanking). Cmem No allows you to automatically change beam current for different lines in the schedule list. If you would like the system to perform a field correction at any time, enter a line of #K in the file name with nothing else (note: if you change the beam current it will automatically perform a Field and Beam Position correction). This allows for a field correction to be performed before continuing the write (see page 84 of the manual for more). To exit out of Insert Schedule mode, press Esc.

- Perform a field correction by type “F” (press f on the keyboard). Before doing this, write down the z-position of the stage where your sample is focused. The stage will drive to perform a field correction. You will be prompted with the query “Check Contrast and Brightness Exe Y/N?” Enter Y. The system will perform a field correction. Once its done, enter N if you don’t want to repeat the field correction (Hint: if the values of Width ATTX and Y are greater than 10 percent away from 8000, you might want to repeat the field correction, see Fig. 19).
- Manually set the z-coordinate back to the correct value for your sample.



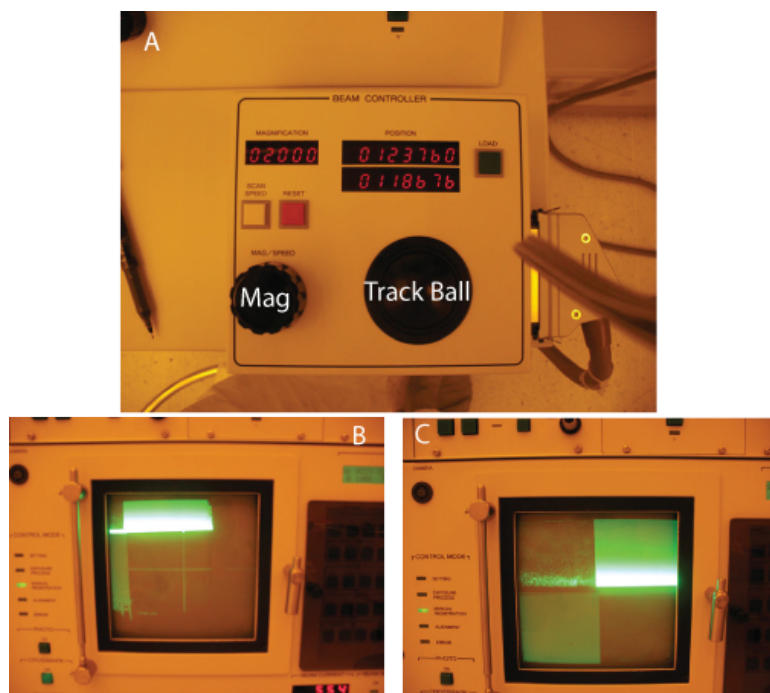


Figure C.21: Beam controller and process for aligning chip with the Registration Marks created in Job 1.

button. The stage will move to Marker B. Perform the same steps to align Mark B with the cross hairs. Press LOAD when you are happy with the alignment (make sure the magnification is the same as when you pressed LOAD for Marker A, otherwise the system won't accept the LOAD button). The system will then perform another field correction and move back to Marker A to repeat the process. This continues until the alignment is so good that you no longer move the Track Ball any more to align the markers with the cross hairs. If you move the ball AT ALL, the system will repeat the process until you press LOAD without moving the Track Ball at all. If, at any time, you want to stop the process, press and hold the SCAN SPEED button for 3 seconds.

- Once the Registration is complete, the program will continue and write the .CON file you create in Job 1.
- Once the Exposure is complete, the stage will return the the FC.

To unload the sample, you should

- Make the the sample is in the Exchange (EX) Position and the the Exchange Position light in on.
- Close the Isolation Valve.
- Make sure the loadlock is still at adequate transfer pressure by the green EVAC light is on and not flashing. If it is not, press the Vacuum Toggle Button to EVAC and wait for the green light to stop flashing.
- Switch the Door Control Button to Open.
- Push transfer rod in towards the sample. Once it is all the way extended into the chamber, screw in the rod to the transfer plate. The upper white line in Fig. 9 should disappear when the screw in all the way in. Do not torque the plate at all.
- Retract the transfer rod and sample plate completely.
- Switch the Door Control Button to Close.
- Vent the chamber and take you sample and the sample plate out of the loadlock.
- Close loadlock and EVAC.

Need to find something? See Figures 22 and 23.

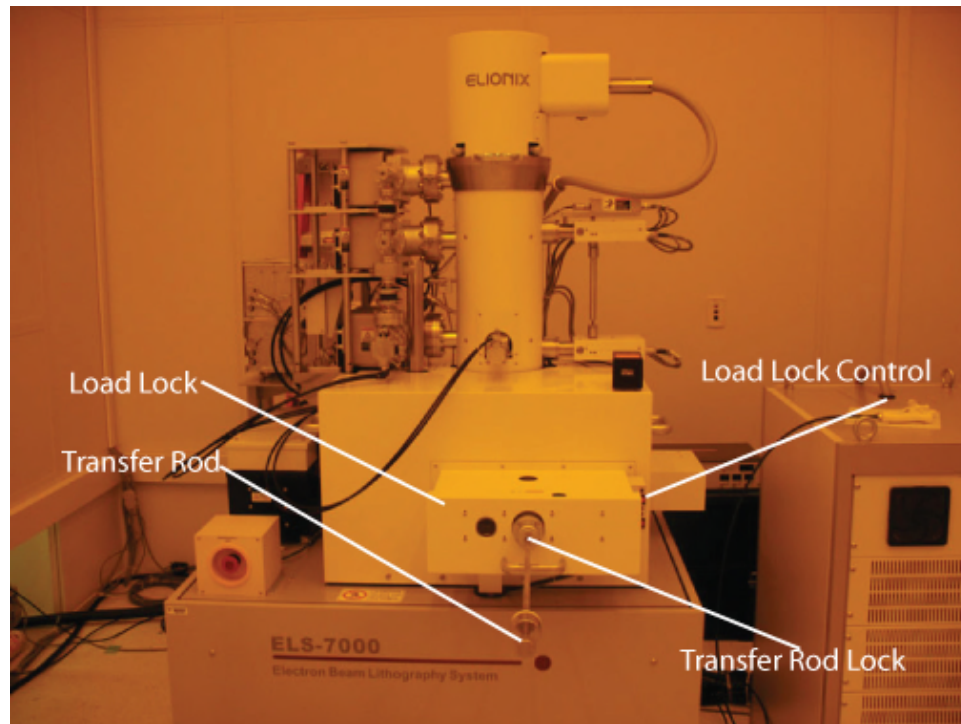


Figure C.22: Things around the load lock.

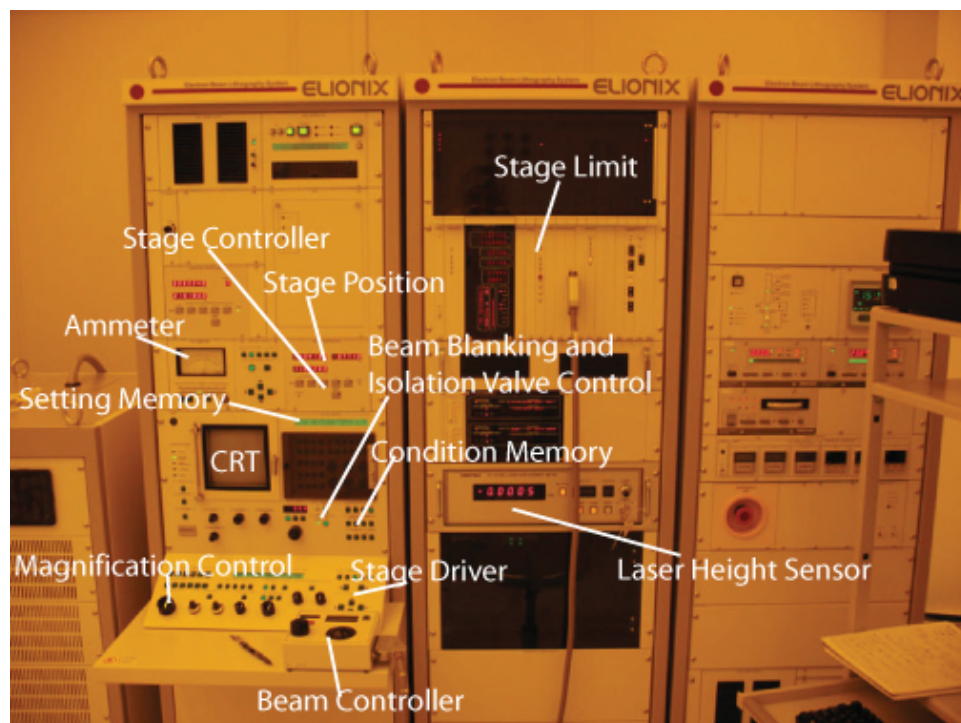


Figure C.23: Things around the Control Panel.

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